COMMON EUROPE
CONGRESS 2026

14 - 17 June
Lyon, France

The largest conference in Europe
for solutions around IBM Power (IBM i, AIX, Linux) & IBM Storage

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Welcome to Lyon, France
and the 2026 Common Europe Congress

Bienvenue à Lyon, en France,
et au Congrès de Common Europe 2026

Power Processor Roadmap:
Power11,
Memory Architecture,
Enterprise AI, and
Chiplets

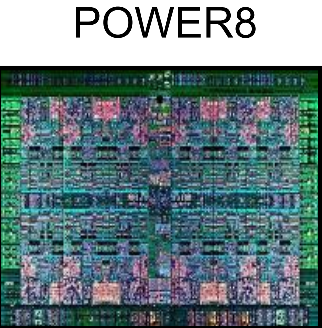
William Starke
IBM Distinguished Engineer
POWER Processor Chief Architect

IBM i

IBM

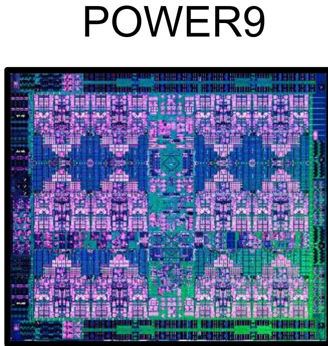
IBM Power Processor Roadmap
Continuous Platform Innovation and Leadership

POWER8



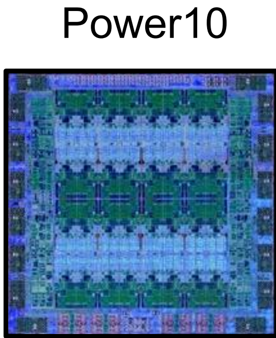
Powerful SMT8 Core
Enterprise Scaling
Big Data Optimized
Agnostic Memory

POWER9



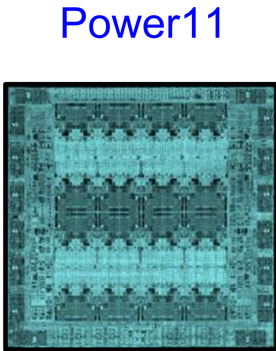
Modular Core Design
Accelerator Attach
(NVlink, OpenCAPI)
Data Plane Bandwidth
DDR & CDIMM Memory

Power10



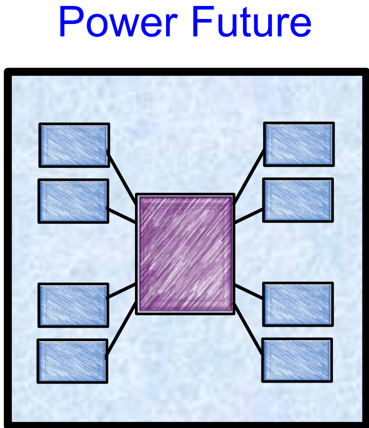
Core / Thread Strength
Socket Performance
In-Core AI Acceleration
Efficiency / Sustainability
HW Accelerated Security

Power11

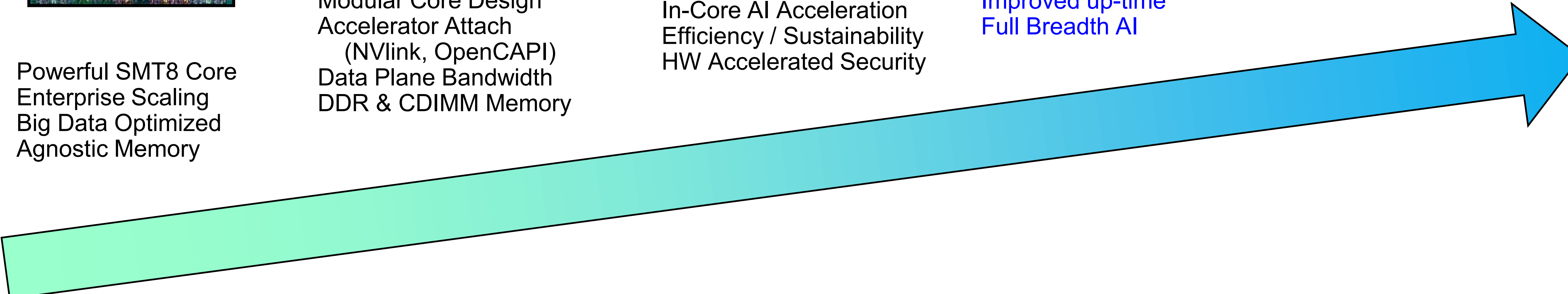


Core / Thread Strength
Socket Performance
Enterprise Scaling
Energy Optimization
Improved up-time
Full Breadth AI

Power Future



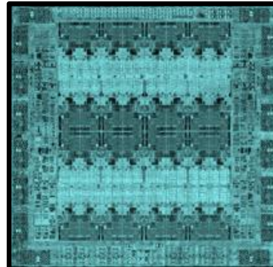
(Under development)



Information is forward looking and plans are subject to change based upon IBM's discretion

Power11: Full Stack Innovation and Cross-Optimization

Processor Architecture
Socket-level Packaging
Semiconductor Technology



Improved Thread, Core, Capacity
ISC Silicon Layer: Energy Optimization
Samsung Foundries Enhanced 7nm

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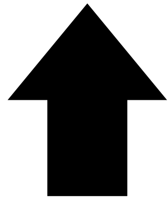
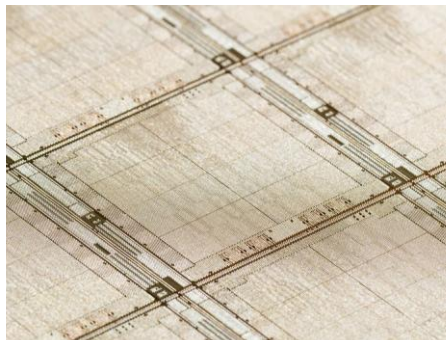
From Power10 to Power11…

2-Socket System: 50% More Cores @ Higher Clock Speed

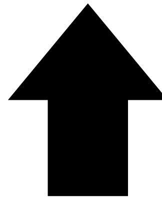
Largest System: 4.0 GHz ➡ 4.3 GHz (with More Cores)



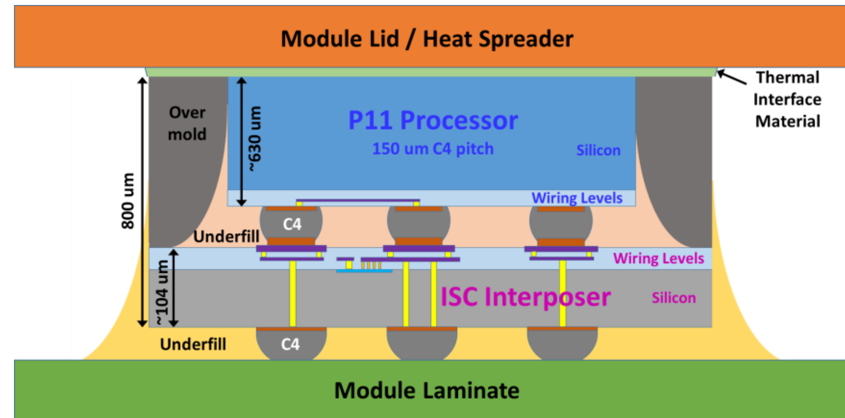
Density vs **Speed**



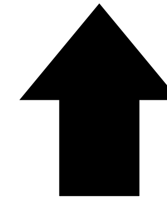
Samsung Foundries
5nm vs **Enhanced 7nm**?



2.5D ISC Architecture



Samsung iCube Si Interposer technology



Chip Architecture

From Power10 to Power11…

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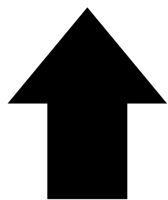
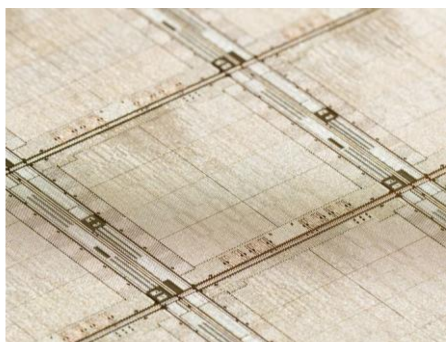
Largest System: 4.0 GHz ➡ 4.3 GHz (with More Cores)



Density vs **Speed**



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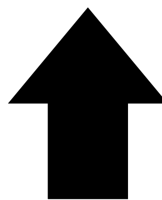
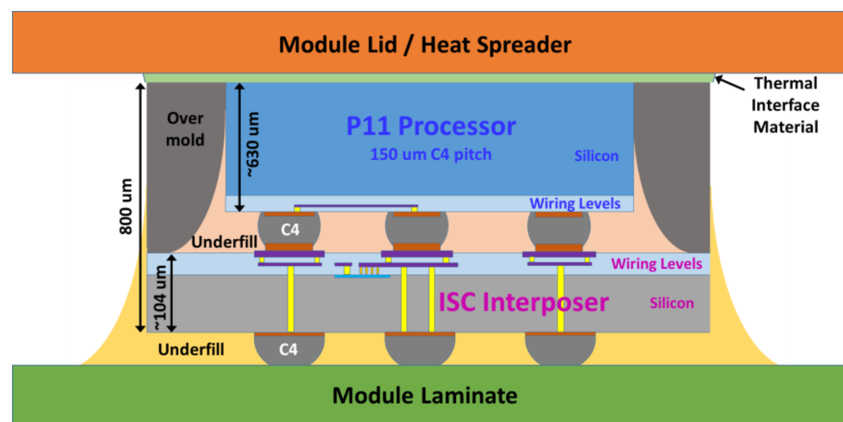
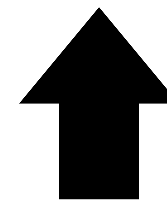


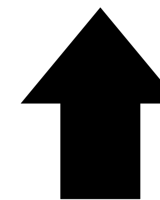
2.5D ISC Architecture



Samsung iCube Si Interposer technology



Chip Architecture



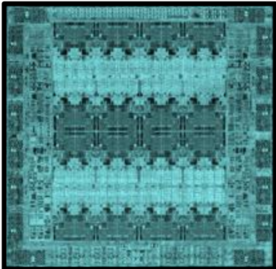
System Thermal
Innovation

Power11: Full Stack Innovation and Cross-Optimization

Energy / Thermal Infrastructure

Processor Architecture
Socket-level Packaging
Semiconductor Technology

Advanced Cooling Technology



Improved Thread, Core, Capacity
ISC Silicon Layer: Energy Optimization
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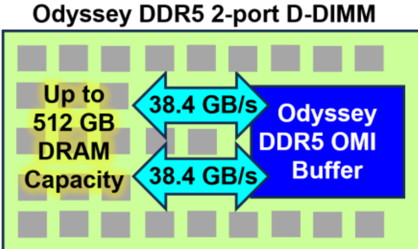
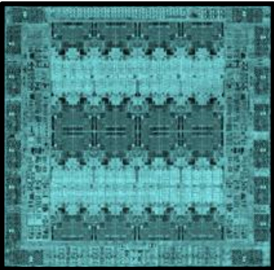
Power11: Full Stack Innovation and Cross-Optimization

Memory Architecture
Energy / Thermal Infrastructure



Agnostic, 3x Pipes, 2x Capacity
Advanced Cooling Technology

Processor Architecture
Socket-level Packaging
Semiconductor Technology



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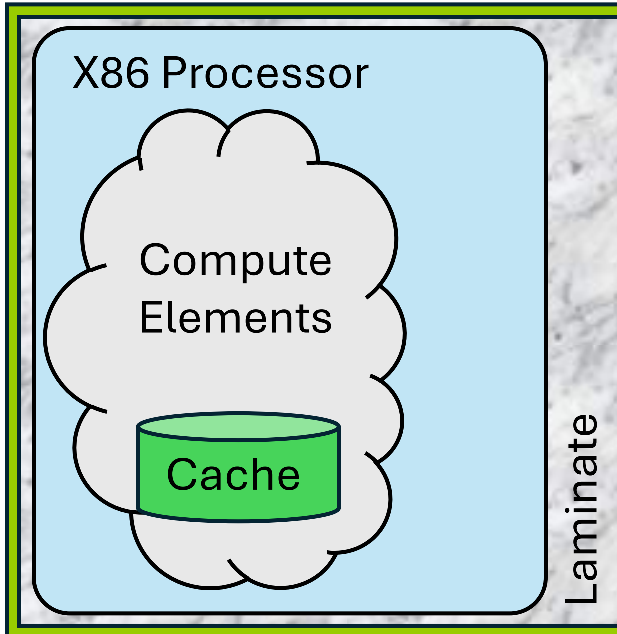
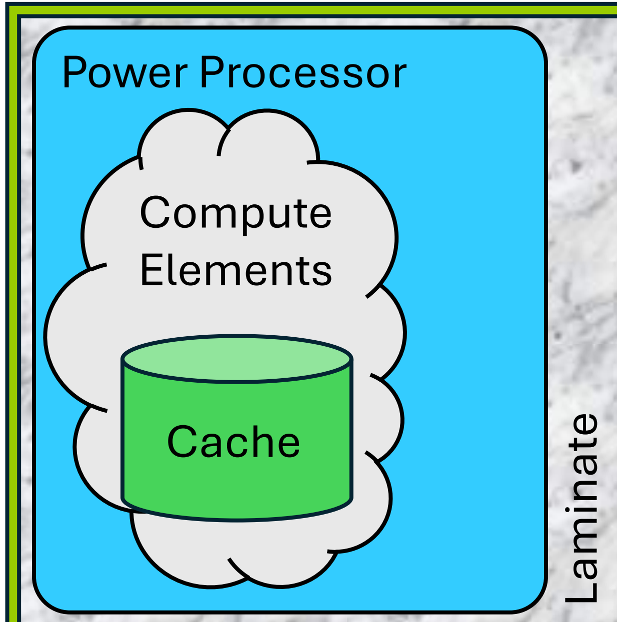
Advantages of Power's OMI Memory Architecture



Starting Point (Unbalanced):

- Too many Cores
- Cores are Weak
- Not enough Cache per Core

→ Unnecessarily high traffic rate to memory



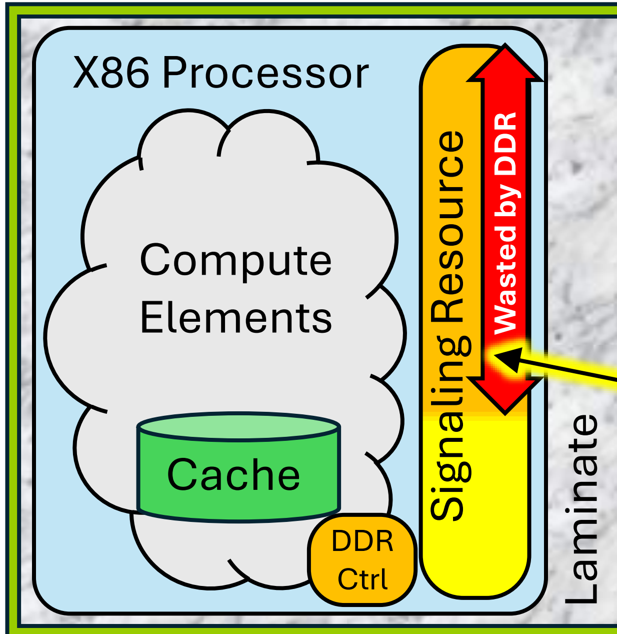
Starting Point (Advantaged):

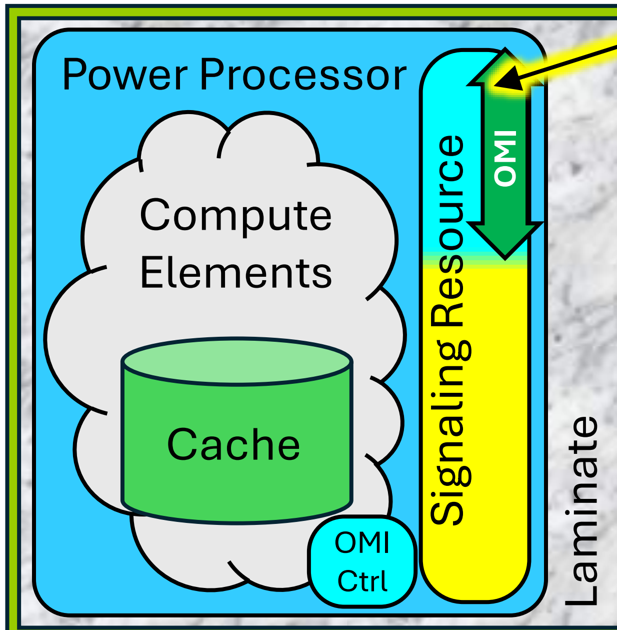
- Fewer Cores
- Each Core is Powerful
- Robust Cache per Core

→ Reduced traffic rate to memory

Advantages of Power's OMI Memory Architecture

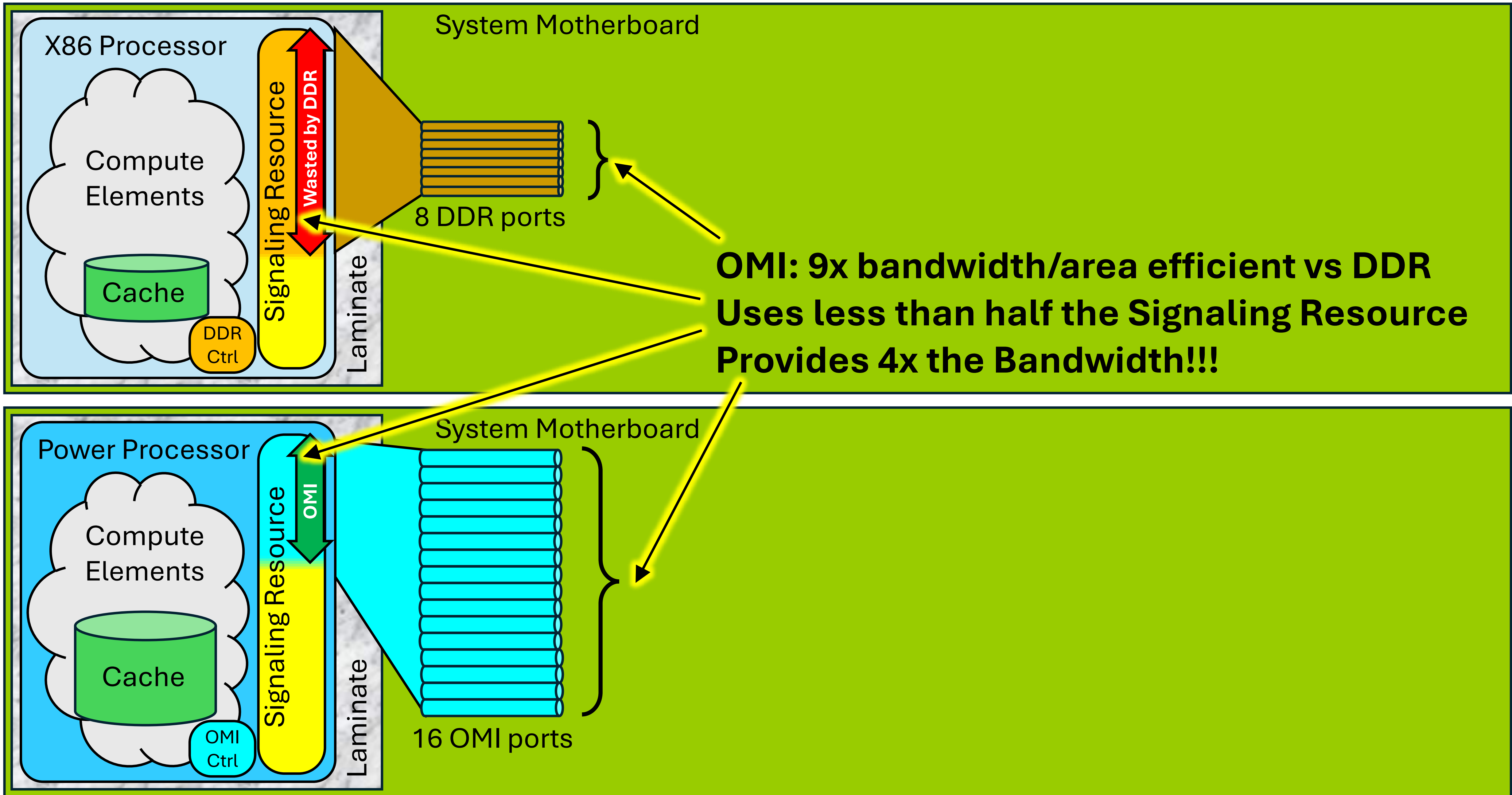
Advantages of Power's OMI Memory Architecture





OMI: 9x bandwidth/area efficient vs DDR
Uses less than half the Signaling Resource

Advantages of Power's OMI Memory Architecture



Advantages of Power's OMI Memory Architecture

X86 Processor

Compute Elements

Cache

DDR Ctrl

Signaling Resource

Wasted by DDR

Laminate

System Motherboard

8 DDR ports

OMI: 9x bandwidth/area efficient vs DDR

Uses less than half the Signaling Resource

Provides 4x the Bandwidth!!!

Power Processor

Compute Elements

Cache

OMI Ctrl

Signaling Resource

OMI

Laminate

System Motherboard

16 OMI ports

DDR Signaling

- Structured to communicate with DRAM semiconductor technology
- Extremely primitive compared to modern signaling architectures
- Terribly wasteful of signaling resource
- Industry seems stuck with it

OMI Signaling

- Modern SERDES architecture for latest processer technology
- Area efficient, high bandwidth, low latency, low power
- Industry has evolved to SERDES for everything except memory
- IBM's SERDES is even better than industry's (decades of innovation)

Advantages of Power's OMI Memory Architecture

X86 Processor
Compute Elements
Cache
DDR Ctrl
Signaling Resource
Wasted by DDR
Laminate
System Motherboard
8 DDR ports
DDR port
DIMM Connector

DDR Signaling
- Wasted Processor signaling resource
- **Wasted motherboard wiring**
- **Wasted connector resource**

Power Processor
Compute Elements
Cache
OMI Ctrl
Signaling Resource
OMI
Laminate
System Motherboard
16 OMI ports
OMI port
D-DIMM Connector

OMI Signaling
- Efficient Processor signaling resource
- **Efficient motherboard wiring**
- **Efficient connector resource**

Advantages of Power’s OMI Memory Architecture

System Motherboard
X86 Processor
Compute Elements
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8 DDR ports
DDR port
DIMM Connector
Industry Standard DIMM

System Motherboard
Power Processor
Compute Elements
Cache
OMI Ctrl
Signaling Resource
OMI
Laminate
16 OMI ports
OMI port
D-DIMM Connector
OMI Chip
DDR Ctrl
DDR port
OMI D-DIMM

Added OMI Memory Buffer

- Like breaking off piece of Processor and moving it to Memory DIMM
- Enables SERDES signaling
- Contain DDR within DIMM
- Minimal Latency growth

Advantages of Power's OMI Memory Architecture

X86 Processor

Compute Elements

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Signaling Resource

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Power Processor

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16 OMI ports

OMI port

D-DIMM Connector

DDR port

OMI Chip

DDR Ctrl

DDR port

OMI D-DIMM

Added OMI Memory Buffer

- Like breaking off piece of Processor and moving it to Memory DIMM
- Enables SERDES signaling
- Contain DDR within DIMM
- Minimal Latency growth
- **Hierarchical multiplier!!!**

Advantages of Power’s OMI Memory Architecture

X86 Processor
Compute Elements
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DDR Ctrl
Signaling Resource
Wasted by DDR
Laminate
System Motherboard
8 DDR ports
DDR port
DIMM Connector
DRAM Chip
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DRAM Chip
Industry Standard DIMM

Power Processor
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OMI Chip
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OMI D-DIMM

Advantages of Power's OMI Memory Architecture

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DDR port
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DRAM Chip
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DRAM Chip
Industry Standard DIMM x 8
= **8 total DDR ports**

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OMI D-DIMM x 16 = **32 total DDR ports**

Minimizing Fragile DDR Signaling Reliability

Leveraging Robust OMI Signaling Reliability

X86 Processor
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OMI D-DIMM x 16 = **32 total DDR ports**

N+1 Redundancy to Mitigate DRAM Chip Reliability

X86 Processor
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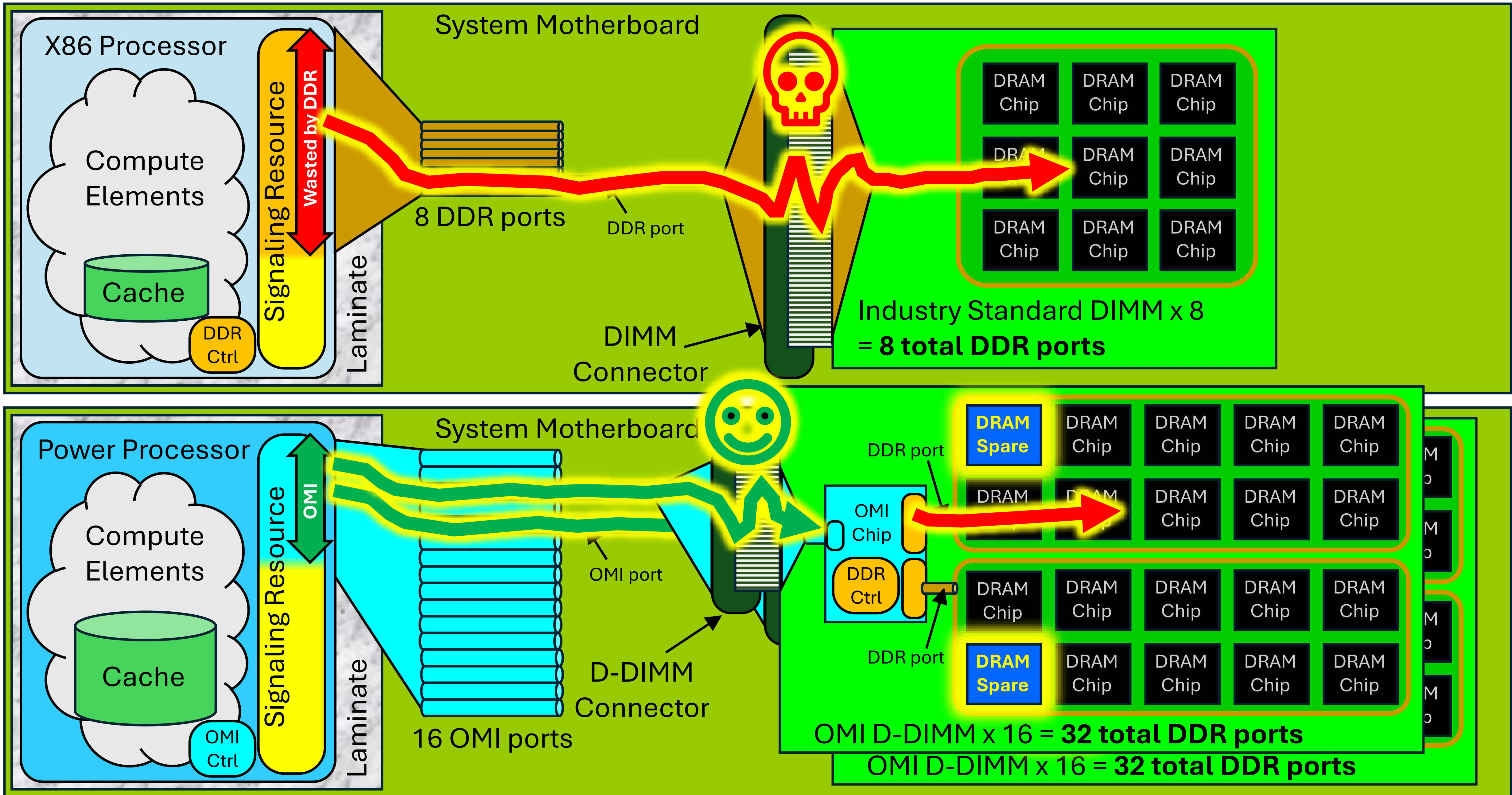
DRAM Chip
DRAM Spare
OMI D-DIMM x 16 = **32 total DDR ports**

Selective Memory Mirroring



Rigid DDR Vintage Processor / Memory Lock-In vs Composability

X86 Processor

Compute Elements

Cache

DDR Ctrl

Signaling Resource

Wasted by DDR

Laminate

System Motherboard

8 DDR por

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DRAM Chip

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Rigid DDR Vintage Processor / Memory Lock-In vs Composability

System Motherboard

X86 Processor

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DIMM Connector

System Motherboard

Power Processor

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OMI port

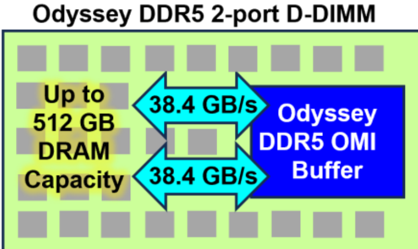
16 OMI ports

D-DIMM Connector

Rigid DDR Vintage Processor / Memory Lock-In vs Composability

Power11: Full Stack Innovation and Cross-Optimization

Memory Architecture
Energy / Thermal Infrastructure



Agnostic, 3x Pipes, 2x Capacity
Advanced Cooling Technology

Processor Architecture
Socket-level Packaging
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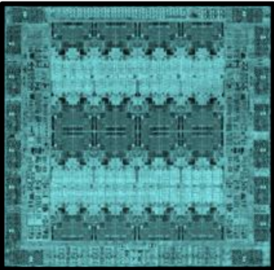

Improved Thread, Core, Capacity
ISC Silicon Layer: Energy Optimization
Samsung Foundries Enhanced 7nm

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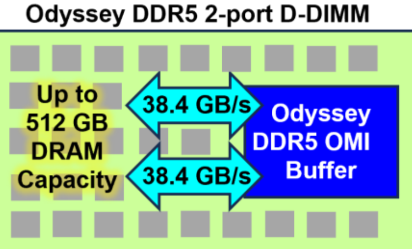
Power11: Full Stack Innovation and Cross-Optimization

Platform Capabilities — Uptime, Energy Mgmt, Security, Resource Groups

Memory Architecture
Energy / Thermal Infrastructure



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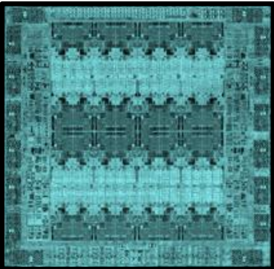

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Power11: Full Stack Innovation and Cross-Optimization

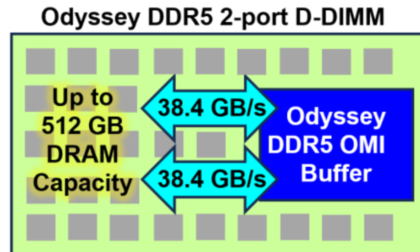
AI Acceleration

Accelerated AI (all systems)
IBM Spyre Accelerator
Optimized for Inference

Platform Capabilities

Uptime, Energy Mgmt, Security, Resource Groups

Memory Architecture
Energy / Thermal Infrastructure



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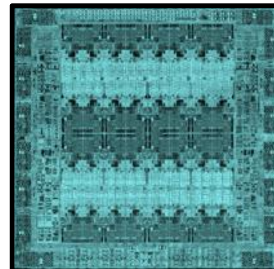

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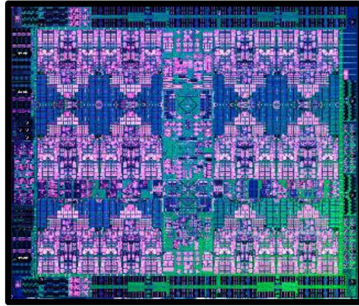
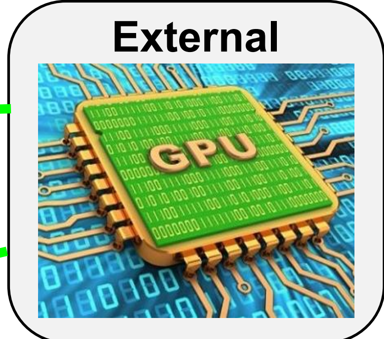
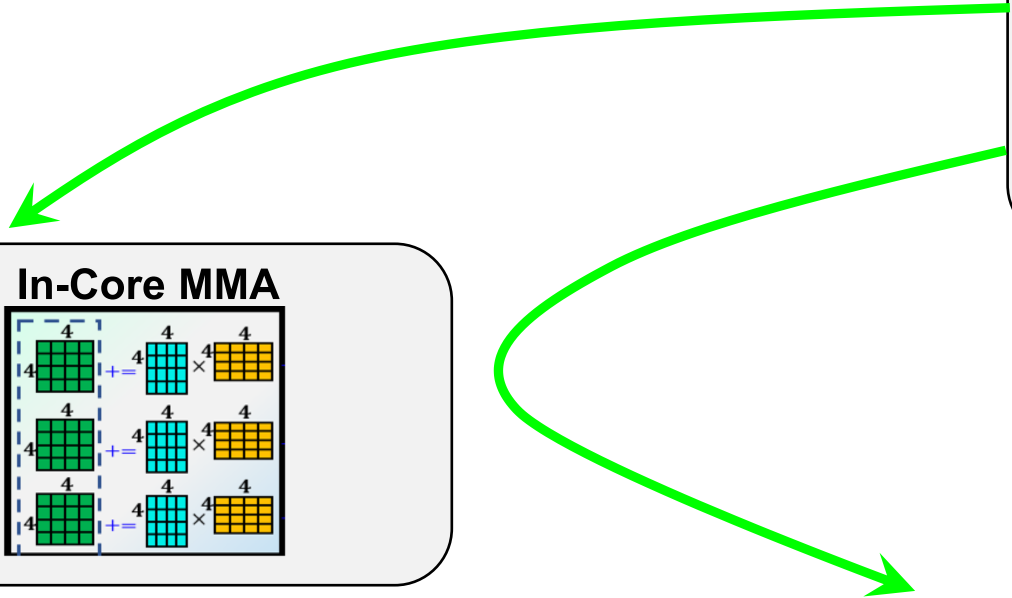
AI Improvements: Accelerated support for Large Models and Model Tuning

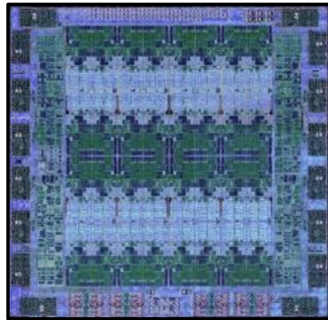
POWER9

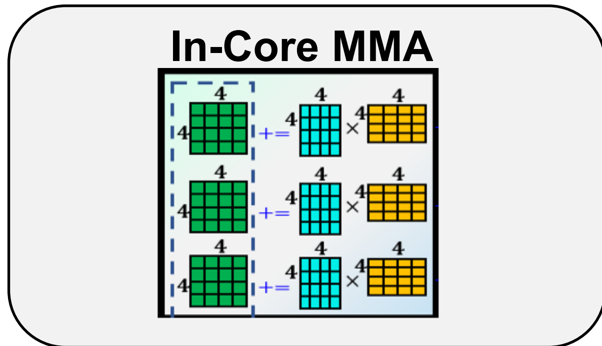






Power10





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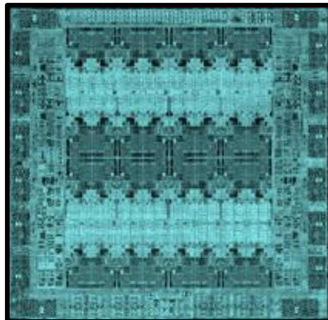
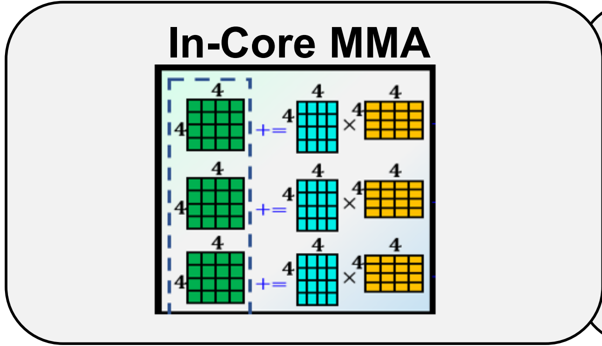
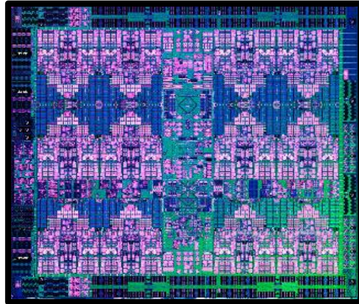
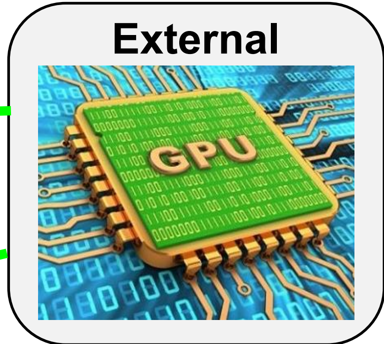


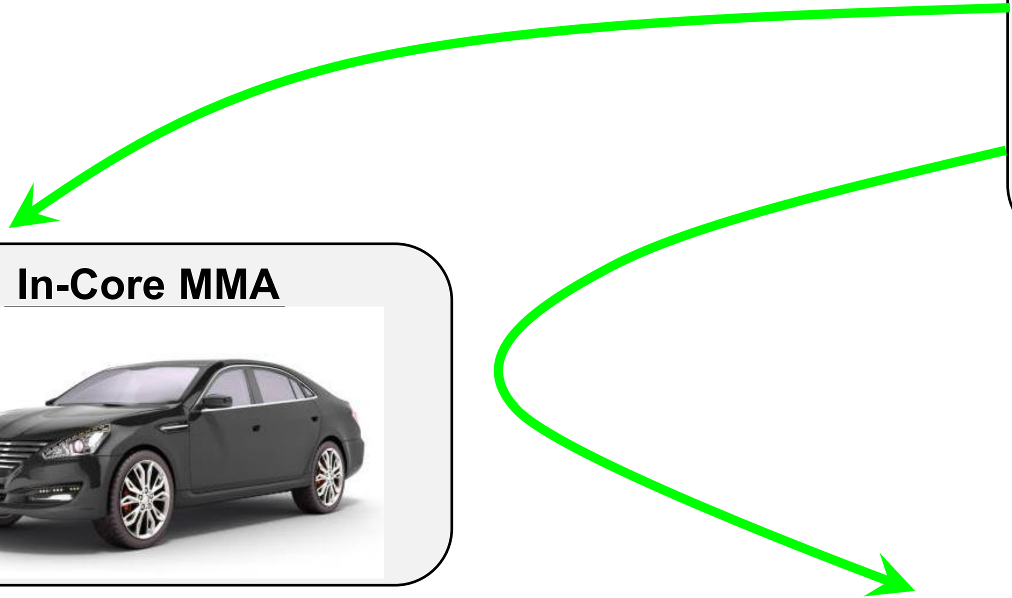


AI Improvements: Accelerated support for Large Models and Model Tuning

POWER9







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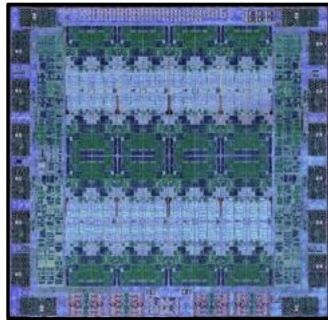

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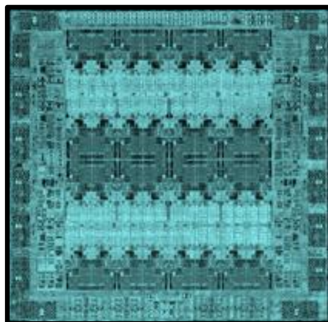
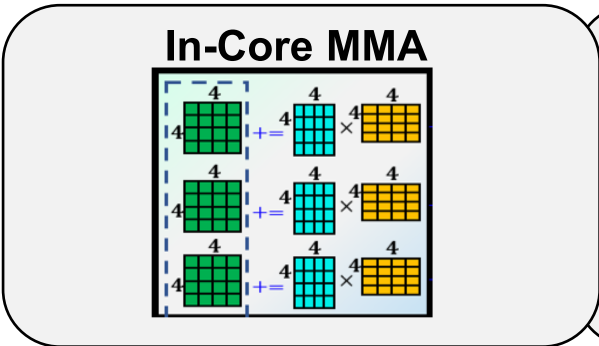
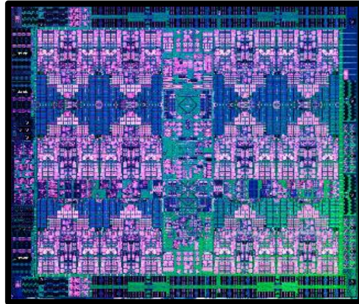
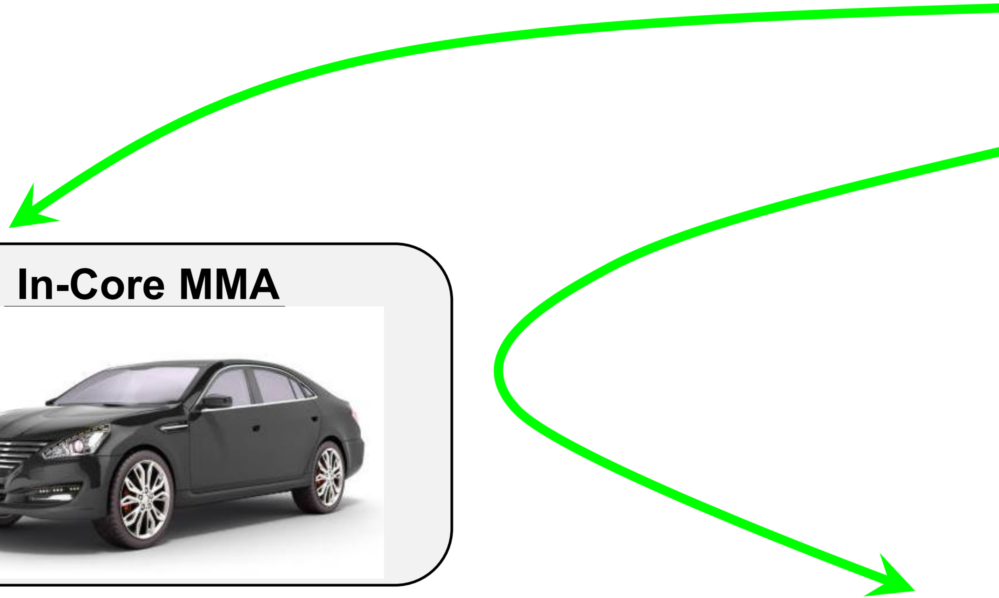




AI Improvements: Accelerated support for Large Models and Model Tuning

POWER9





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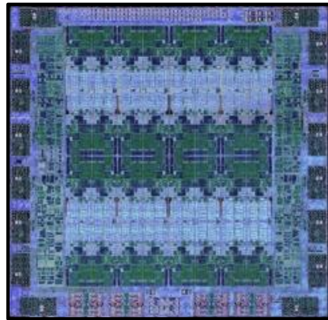

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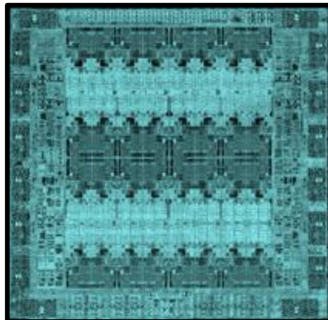
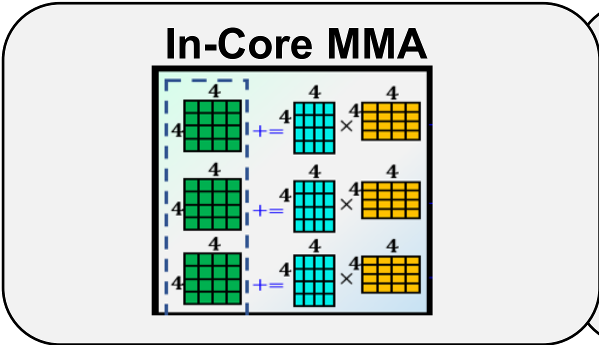
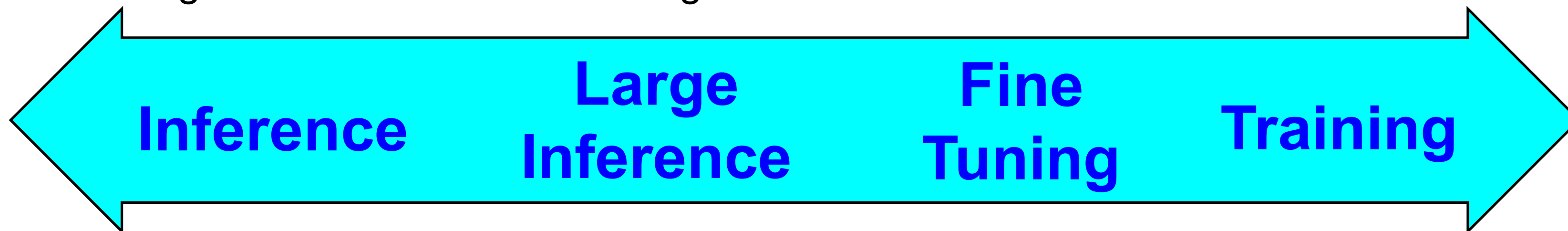




AI Improvements: Accelerated support for Large Models and Model Tuning



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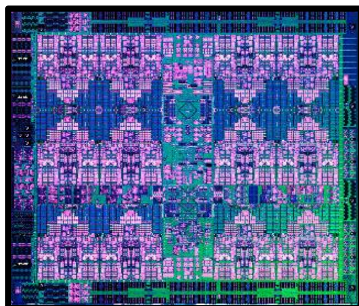

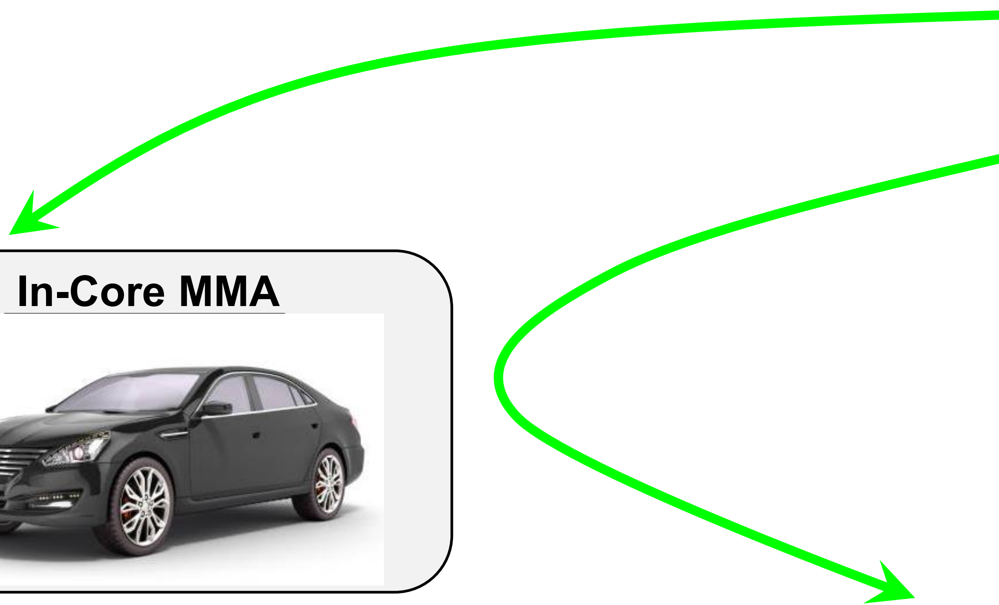

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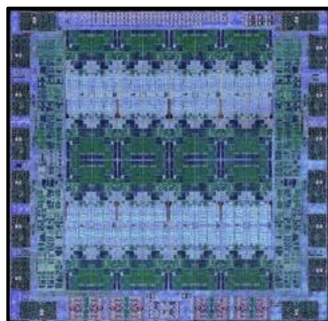

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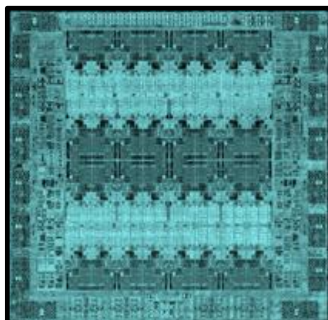


In-Core MMA

External Spyre Accelerator

Power11: Full Stack Innovation and Cross-Optimization

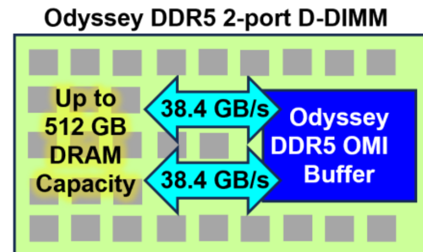
AI Acceleration

Accelerated AI (all systems)
IBM Spyre Accelerator
Optimized for Inference

Platform Capabilities

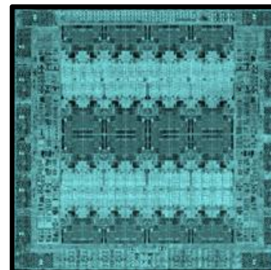
Uptime, Energy Mgmt, Security, Resource Groups

Memory Architecture
Energy / Thermal Infrastructure



Agnostic, 3x Pipes, 2x Capacity
Advanced Cooling Technology

Processor Architecture
Socket-level Packaging
Semiconductor Technology



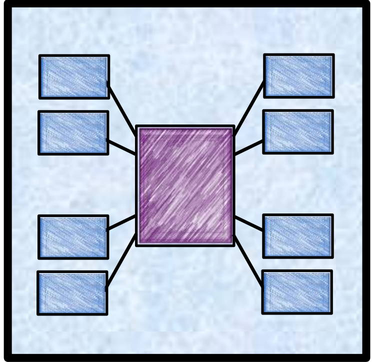
Improved Thread, Core, Capacity
ISC Silicon Layer: Energy Optimization
Samsung Foundries Enhanced 7nm

Information is forward looking and plans are subject to change based upon IBM's discretion

IBM Power Processor Roadmap

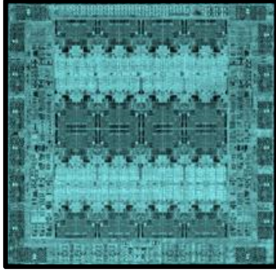
After Power11: Chiplet-based Architecture

Power Future



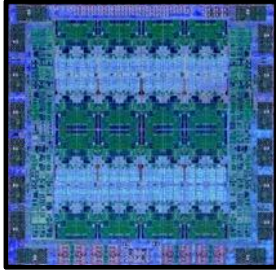
(Under development)

Power11



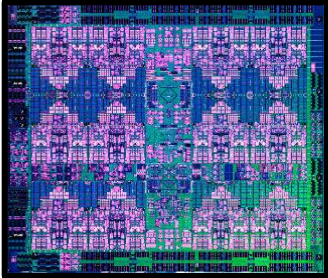
Core / Thread Strength
Socket Performance
Enterprise Scaling
Energy Optimization
Improved up-time
Full Breadth AI

Power10



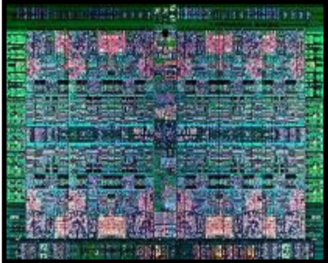
Core / Thread Strength
Socket Performance
In-Core AI Acceleration
Efficiency / Sustainability
HW Accelerated Security

POWER9

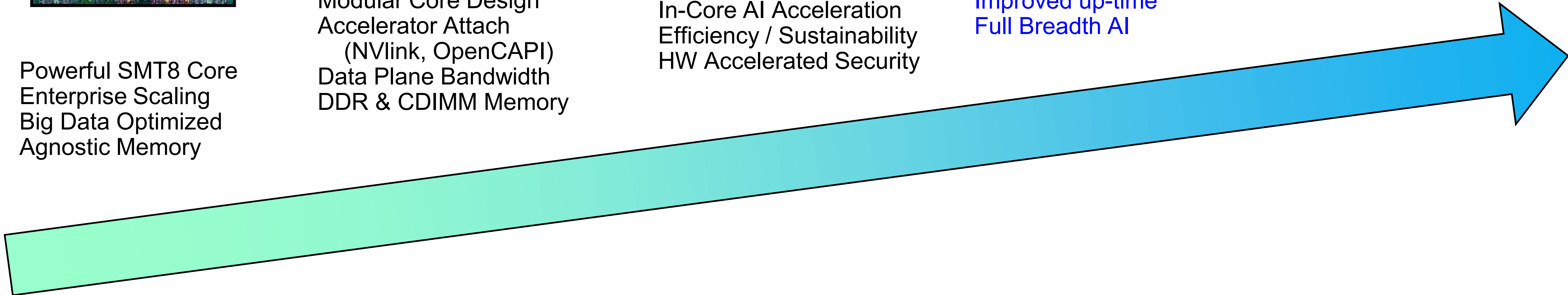


Modular Core Design
Accelerator Attach
(NVlink, OpenCAPI)
Data Plane Bandwidth
DDR & CDIMM Memory

POWER8



Powerful SMT8 Core
Enterprise Scaling
Big Data Optimized
Agnostic Memory



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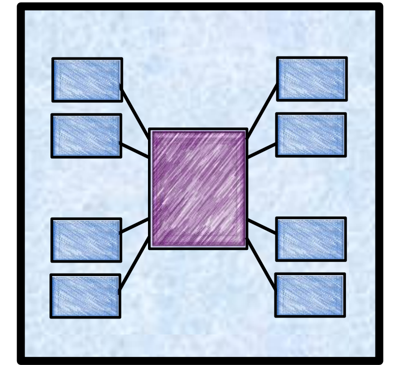
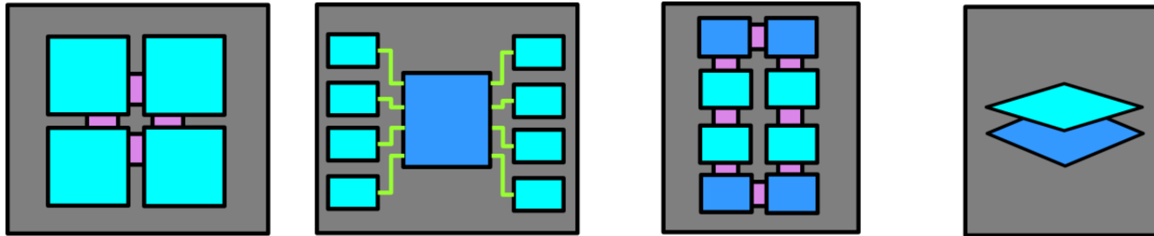
IBM Power Processor Roadmap

After Power11: Chiplet-based Architecture



- Moore's Law Challenge: Silicon Scaling is Slowing
- Industry shift: Leverage Packaging: Chiplets, 3D



- Several years back we assessed for Power …

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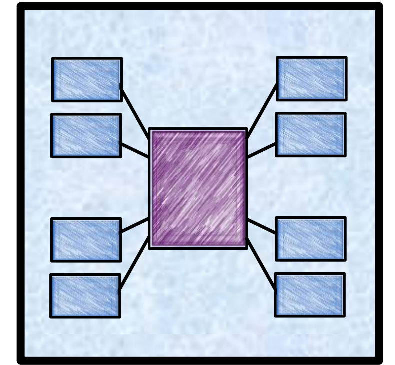
IBM Power Processor Roadmap
After Power11: Chiplet-based Architecture



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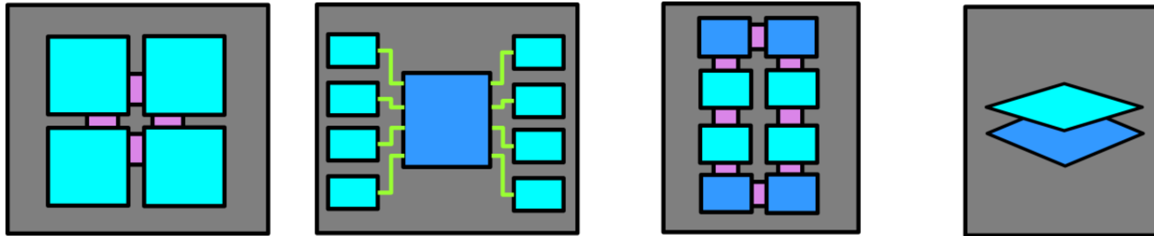

- Several years back we assessed for Power …

System Focus vs Socket Focus

- Full System (Socket-escape) Bandwidth vs Intra-socket Bandwidth
- Distance Signaling vs Low-power (Edge-to-edge) Signaling
- End-to-end Latency vs Computational Density
- Coherent Sharing & Pooled Capacity vs Clustering

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IBM Power Processor Roadmap

After Power11: Chiplet-based Architecture

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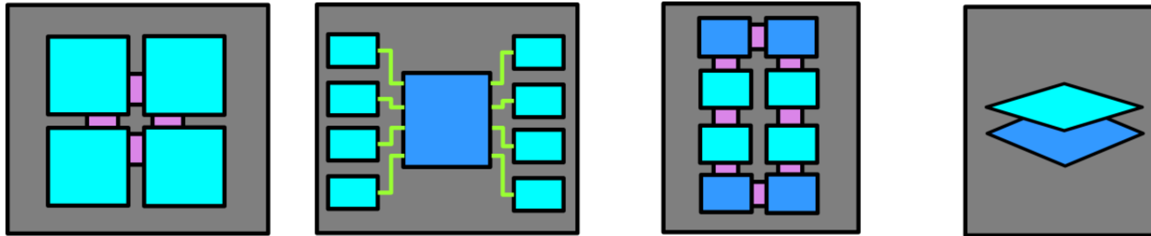

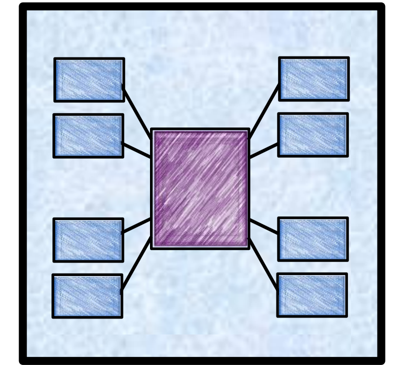

Strong Value for Power Roadmap: Multiple generations into Future

1) 3x Silicon per Socket (small chiplets with room to grow)
2) Manufacturing Yield Synergies
3) Ability to maintain Strong Bandwidth across Chiplets
4) OMI Memory Beachfront Efficiency → Enable High Bandwidth SMP/IO Interfaces
5) Substantial Latency Reduction / Topology Synergy: Continued Robust Scaling
6) Long-term Development Efficiency and Flexibility

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