Welcome to Lyon, France and the 2026 Common Europe Congress

Bienvenue à Lyon, en France, et au Congrès de Common Europe 2026

Power Processors & IBM i

A Brief History of the Past 25 Years

William Starke
IBM Distinguished Engineer
POWER Processor Chief Architect

IBM

Who is the guy talking to you?

me, 15 years younger

- Chief Architect for Power microprocessors

- IBM Distinguished Engineer:
  expert in multiprocessor coherence protocol and transport, data plane, system scaling, cache & memory architecture, and I/O & accelerator attach architecture

- 30 years in Power microprocessor team

- Z Mainframe & Power hardware performance

- Joined IBM Poughkeepsie, NY 1990
  Moved to Austin, TX 1994

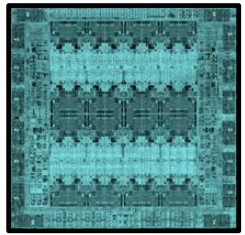

photo of Power11 chip
18 billion transistors
about 1 sq. inch in size

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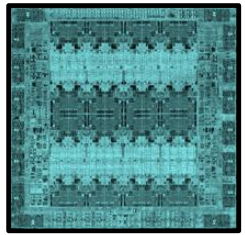

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- College intern at small, mid-Michigan IT consulting firm

  Experienced the arrival of a newborn AS/400 in 1988

  I never imagined I'd one day create the engine inside

IBM i Before Power: A Pre-History

The Origins of Today's Computational Architectures

1964 IBM S/360

z17
Mainframe

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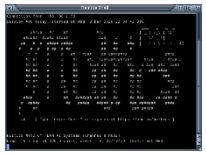

1969 Multics

1973 Unix v4

z17
Mainframe

AIX Linux

Unix

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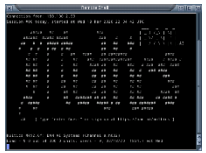

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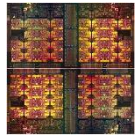

Intel
Sapphire
Rapids

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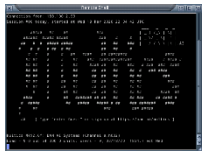

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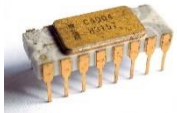

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1978 Intel 8086

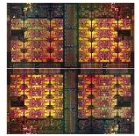
1974 CPM

1981 DOS

1985 Windows

z17
Mainframe

Unix



Intel
Sapphire
Rapids

Microsoft
Windows

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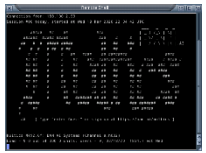

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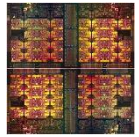

Intel Sapphire Rapids

1974 CPM

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1985 Windows

Microsoft Windows

1978 System 38

1988 AS/400

IBM i

IBM i Before Power: A Pre-History

Most Modern, Most Innovative Platform Architecture ever Created

1964 IBM S/360

1971-1975 IBM "Future Systems" Project

Bold New Architecture: Intended Successor to the S/360

- "Super-CISC", SW Development Productivity Focus
- Multiple Abstraction Levels: Layered Architecture
- Single-Level-Store: Persistent Object-oriented Representation
- Integrated Function: Operating System / Database
- Exotic Hardware: e.g. Wafer Scale Integration

Over-Ambitious, and Lacking in S/360 SW Migration Path

- Killed the Poughkeepsie Large System
- Killed the Endicott Medium System
- The Rochester Small System Inspired the S/38 and AS/400

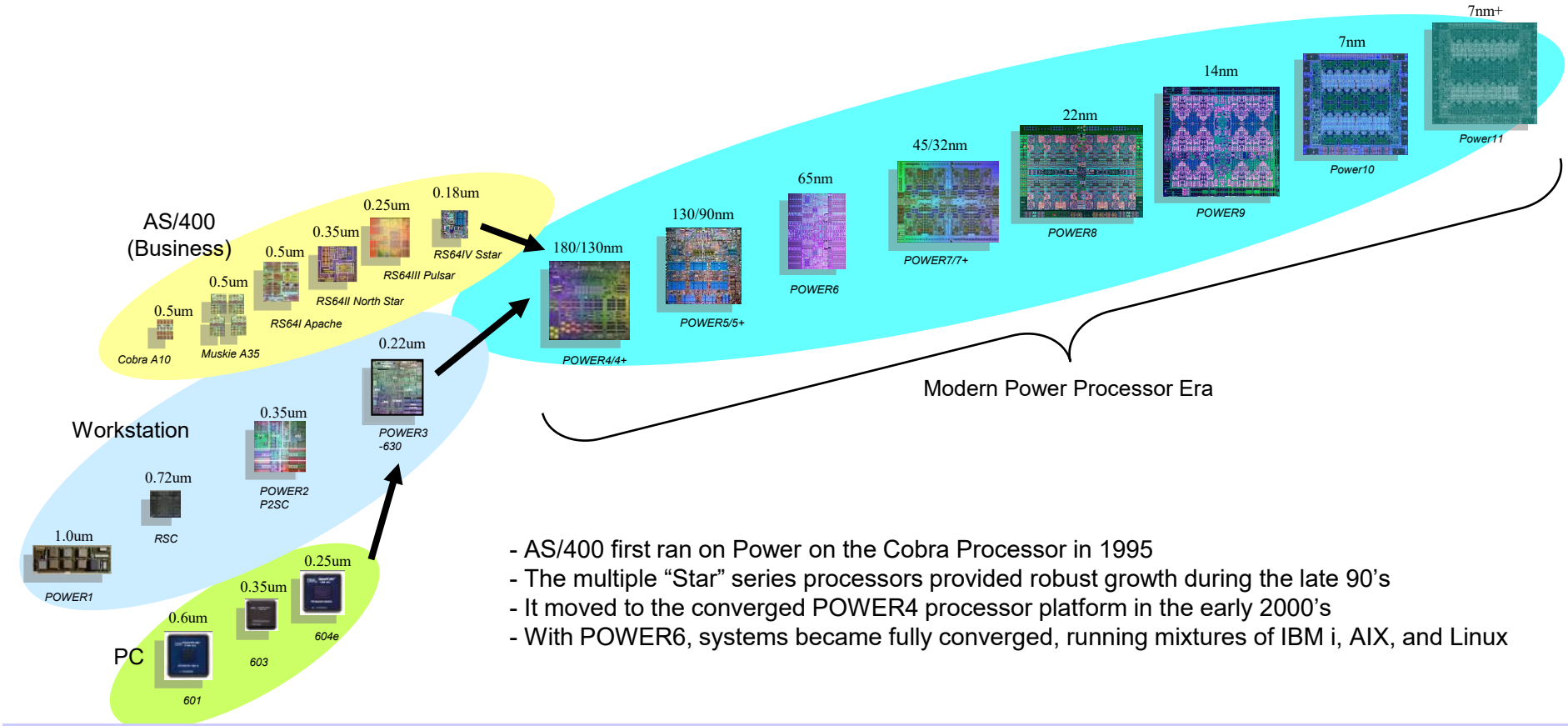
1978 System 38

IBM AS/400

1988 AS/400

IBM i

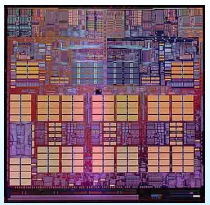
Marriage of IBM i and Power



- AS/400 first ran on Power on the Cobra Processor in 1995
- The multiple “Star” series processors provided robust growth during the late 90’s
- It moved to the converged POWER4 processor platform in the early 2000’s
- With POWER6, systems became fully converged, running mixtures of IBM i, AIX, and Linux

Modern Power Processor History

POWER4/4+



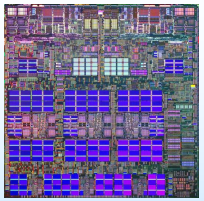
180/130nm SOI

2-core
ST

Powerful Core
Glue-less SMP
eDRAM Cache
Elastic I/O
Commercial/HPC
Z-inspired RAS
Buffered Memory

2001/2003

POWER5/5+



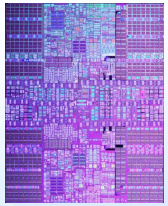
130/90nm SOI

2-core
SMT2

Stronger Core
Enhanced Scaling
Larger SMP
Bandwidth Boost
Integrated MC
Virtualization

2004/2005

POWER6/6+



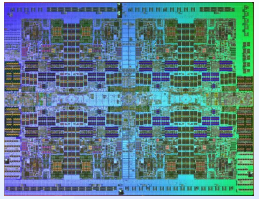
65nm SOI

2-core
SMT2+

Stronger Core
Scaling Boost
Bandwidth Boost
VMX, DFP
Instruction Restart
Protection Keys

2007/2008

POWER7/7+



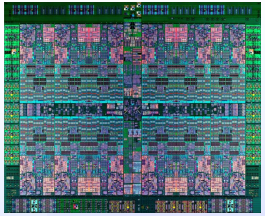
45/32nm SOI

8-core
SMT4

Multi-Core
eDRAM Cache
Energy Mgmt
Mem Bandwidth
Accelerators

2010/2012

POWER8



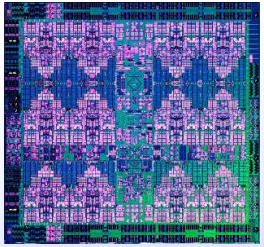
22nm SOI

12-core
SMT8

Stronger Core
Transactional Mem
Centaur Memory
Bandwidth Boost
Scaling Boost
Integrated PCI G3
CAPI Attach

2014

POWER9



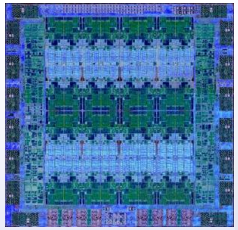
14nm SOI

12/24-core
SMT8/SMT4

Modular Core
Direct-Attach Mem
Bandwidth Boost
Scaling Boost
PowerAXON Attach
Integrated PCI G4
NVLink / OpenCAPI

2018

Power10



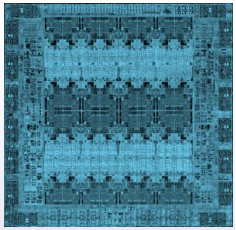
7nm Bulk

15/30-core
SMT8/SMT4

Stronger Core
AI-optimized ISA
OMI Memory
Energy Efficiency
HW Security
Integrated PCI G5
Memory Clustering

2021

Power11



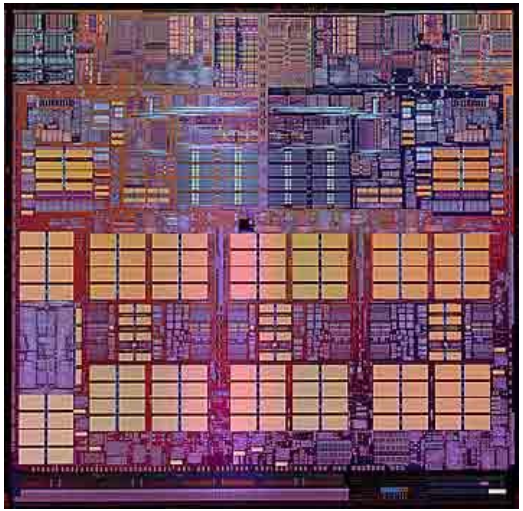
7nm+ Bulk

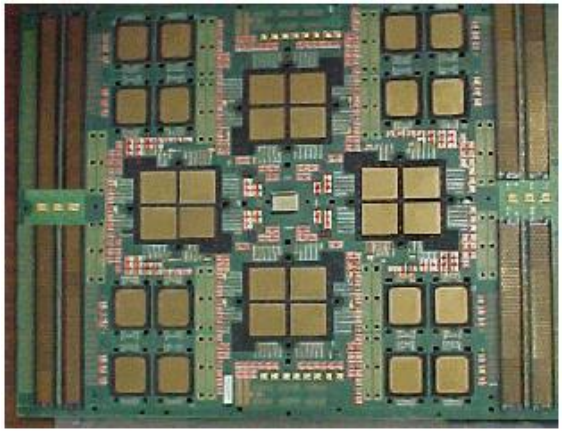
16/32-core
SMT8/SMT4

Stronger Core
Full Breadth AI
OMI DDR5 Opt
Energy Optimized
Quantum-Safe
Improved Uptime
Improved Scaling

2025

POWER4 (2001)

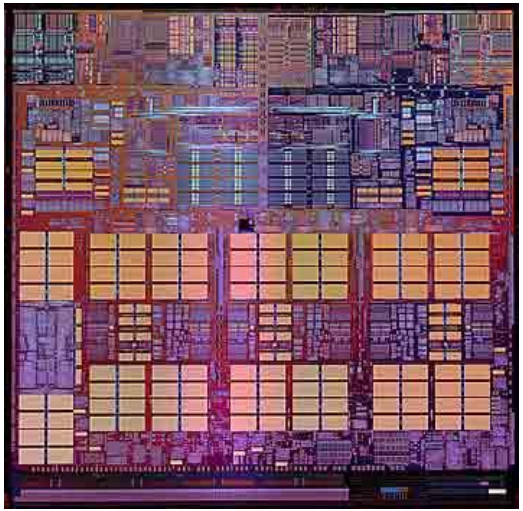


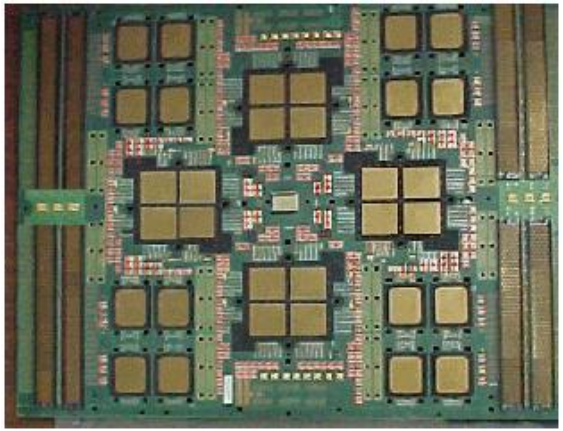


Objectives

- Transform from workstation base
- Boost lagging HPC and commercial UNIX segment to leadership
- Converge AS/400 and UNIX platforms
- Modernize commercial UNIX
- Bring mainframe inspired RAS and Scale

POWER4 (2001)



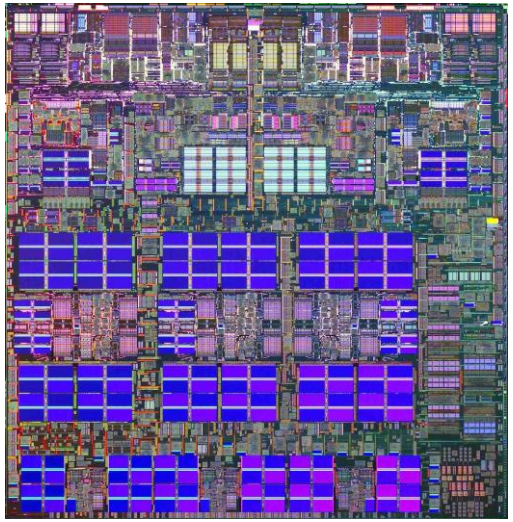


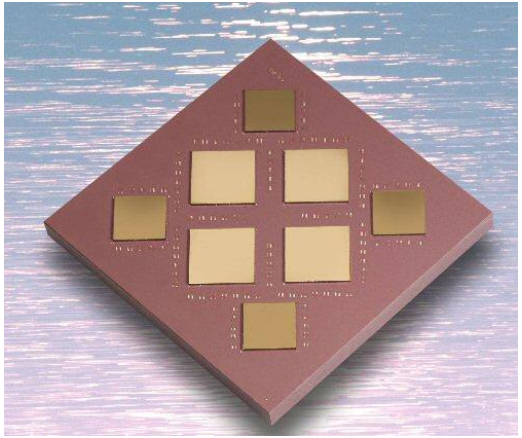
Industry-First Chip Integration

- “System optimized” Dual core chip
- Integrated shared L2 cache
- High frequency (1.3 GHz), Deeply out-of-order, wide superscalar core
- “Elastic” I/O
- Mainframe inspired RAS
- Large 412mm^2 Processor Chip

Mainframe-Inspired Packaging

- Large eDRAM L3 Cache Chips
- Buffered Memory System
- Integrated “Glue-less” SMP Switch Scalable to 16 Processor chips
- Multi-chip Modules (MCMs)
- Large, Complex System Planars

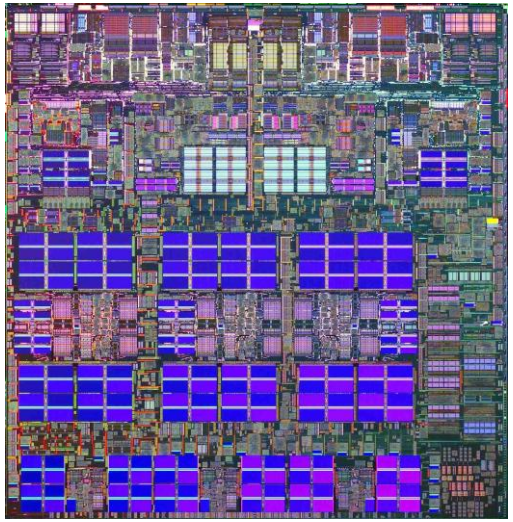


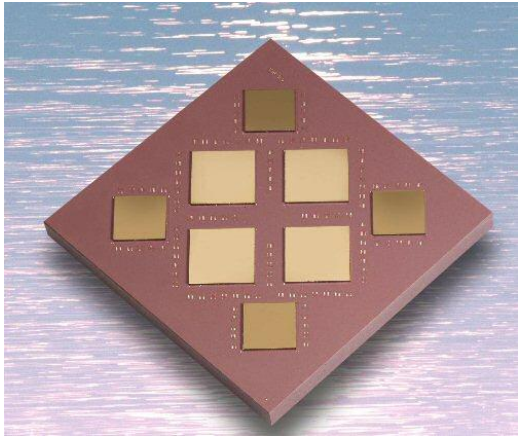


POWER5 (2004)

Objectives

- Build upon tremendous POWER4 success
- Larger, more scalable system
- Improve system modularity
- Bring strong hardware virtualization capability
- Further differentiation against UNIX competitors





POWER5 (2004)

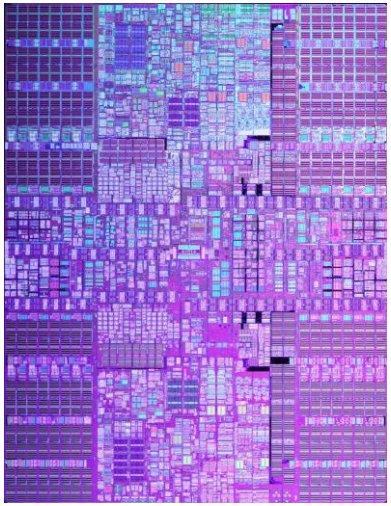
Optimized for Virtualization

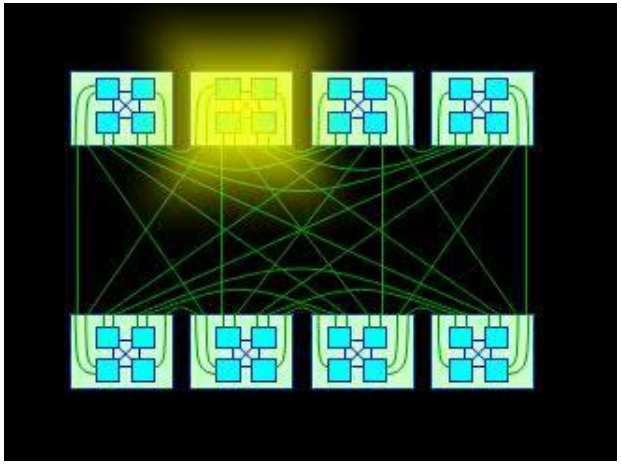
- Built-in hardware virtualization facilities
- Industry first simultaneous multi-threading (SMT) and Glue-less 64-way system provide shared pool of 128 execution threads
- Higher frequency (1.9 GHz), improved out-of-order, wide superscalar core
- Large L3 cache holds multiple working sets
- Large L3 cache as traffic filter → Scaling
- Higher bandwidth interfaces → Scaling

Optimized System Packaging

- 4x memory capacity holds more images
- Industry first integrated memory controller
- 4 Processors + 4 L3 chips on one MCM
- Innovative multi-book 32-chip packaging

POWER6 (2007)

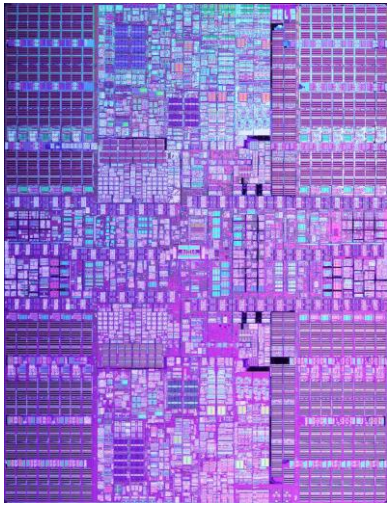


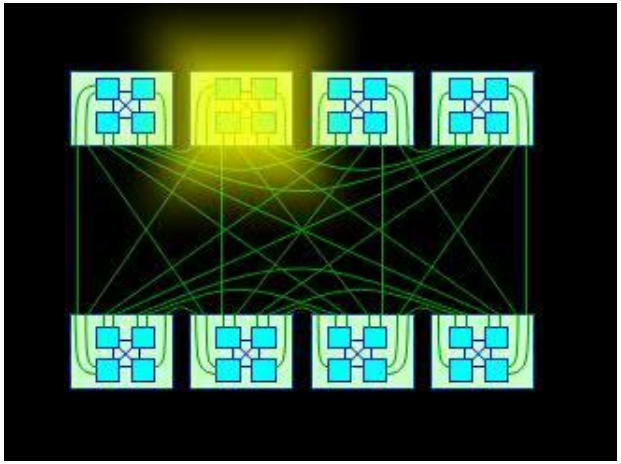


Objectives

- Strong Thread/Core to maximize SW economics, enable differentiated capabilities, and maintain Leadership over emerging X86 competition
- Build upon virtualization success to provide unmatched consolidation capability
- Bring further mainframe-inspired RAS
- Render traditional UNIX competitors irrelevant

POWER6 (2007)



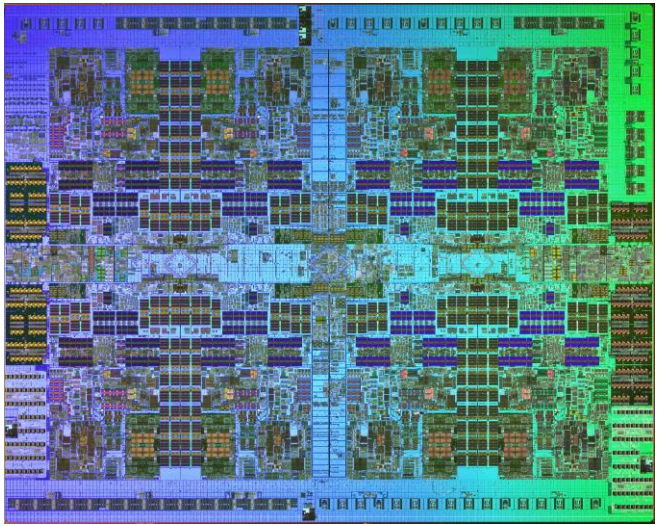


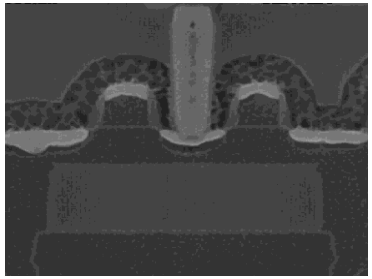
Powerful Core
- Ultra-high Frequency → 5 GHz
- Superscalar
- Altivec extensions
- Decimal Floating Point
- Enhanced SMT

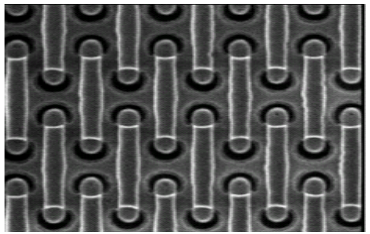
Balanced System
- Large 4M Private L2
- High Speed EI3 SMP and memory interfaces
- Robust SMP Topology
- Dual-scope Coherence
- 3rd Generation L3 and memory buffer chips

Mainframe-Inspired RAS
- Instruction Recovery: Checkpoint/Restart
- Storage Protection Keys
- Active Energy Mgmt
- Live Partition Mobility

POWER7 (2010)



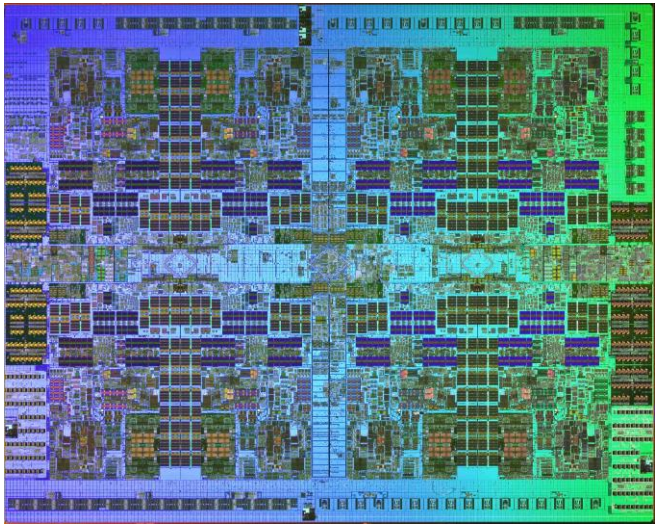


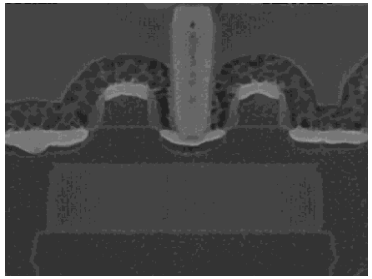


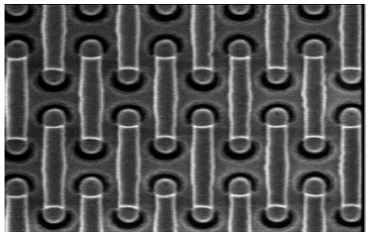
Objectives

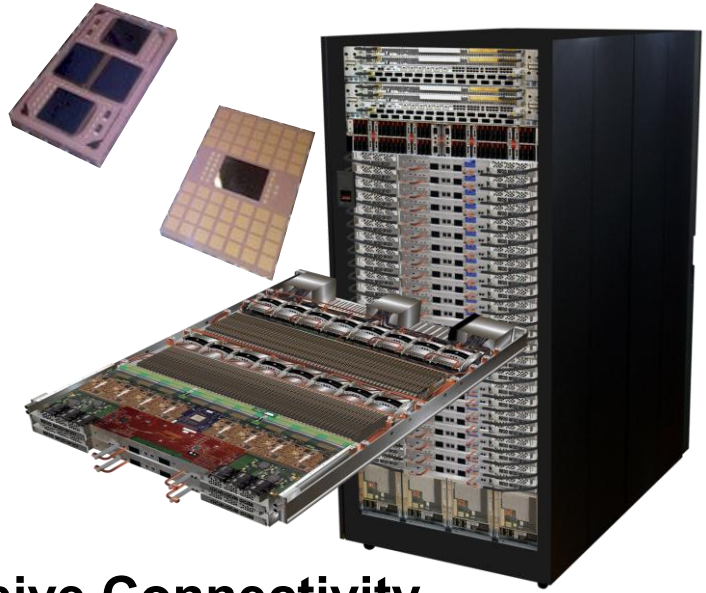
- Massive socket throughput growth to maintain leadership in 2-4 socket space over multi-core X86 competition
- Enhanced dynamic energy mgmt capabilities
- Extreme capacity in large system space to boost consolidation capability
- Massive per-socket HPC throughput and bandwidth
- Integrated clustering support for supercomputing goals

POWER7 (2010)









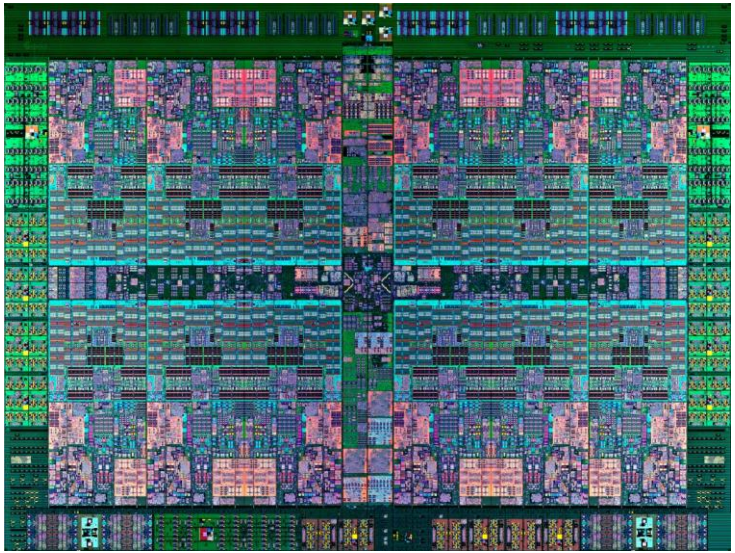
Massive Multi-core Throughput

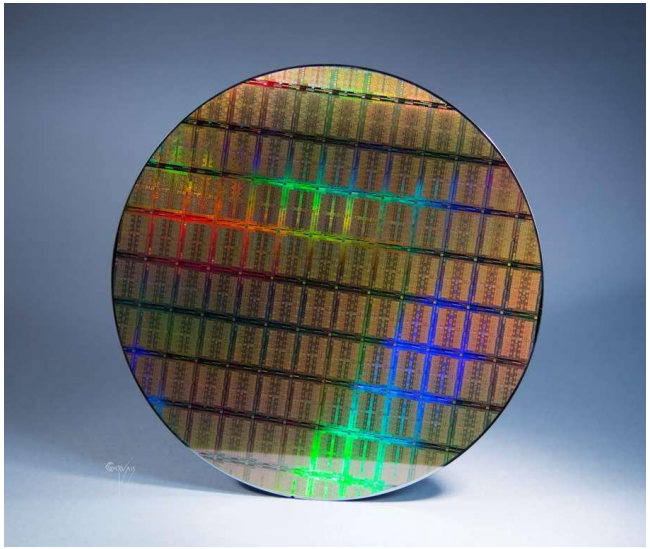
- Up to 8 SMT4 cores / chip (32 threads)
- Superscalar, Deep Out-of-Order
- Industry-exclusive on-chip eDRAM L3
- Cache Hierarchy Innovation: Mixture of eDRAM technology, Hybrid L2/L3 and Aggregated L3 microarchitecture

Massive Connectivity

- 90 GB/s mem bandwidth / socket
- Glue-less 256-core SMP system
- Companion petascale clustering chip
- 500K cores interconnected at sub-microsecond latency with 1.2 PB/s bisection bandwidth

POWER8 (2014)

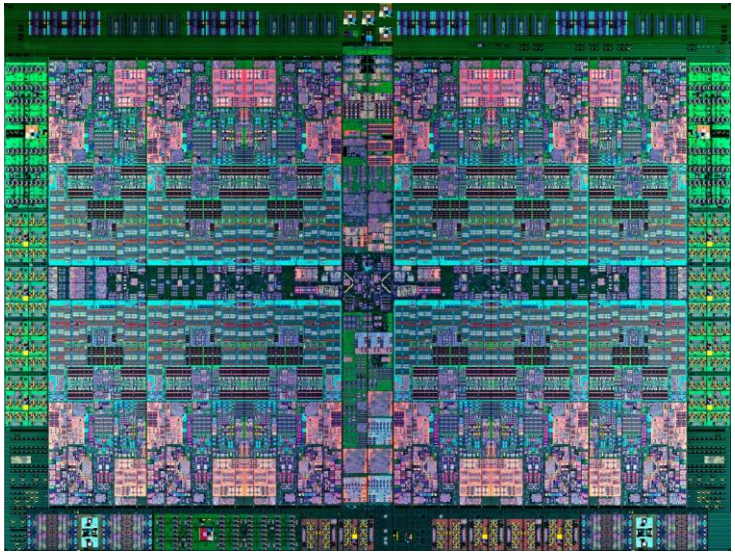


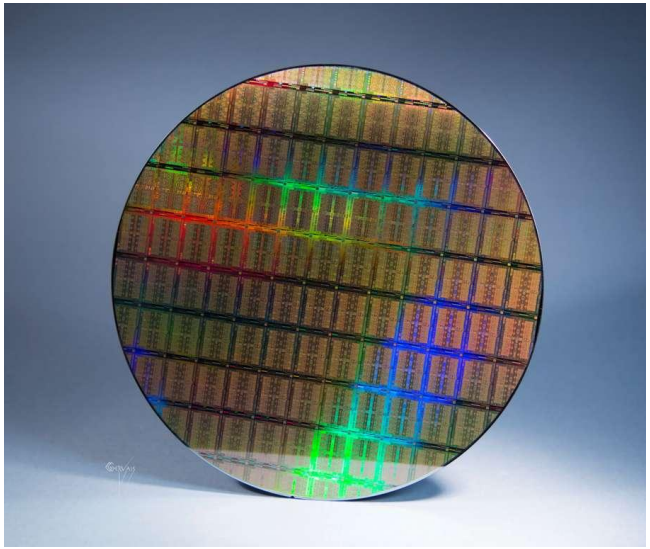


Objectives

- Strong Thread/Core to extend lead over X86
- Enterprise System Scaling
- Strong socket throughput for Scale-out space
- Design to Optimize for Big Data / Analytics
- Leverage/Optimize across IBM HW/SW stack
- Open interfaces to foster multi-partner collaborative innovation.

POWER8 (2014)





Built for Big Data

- 22nm eDRAM, 15 LM
- Java compute assists, TM
- 2x L1/L2/L3 cache per core
- 2x Dataflows
- 230 GB/s mem bandwidth
- 96 GB/s PCI I/O bandwidth

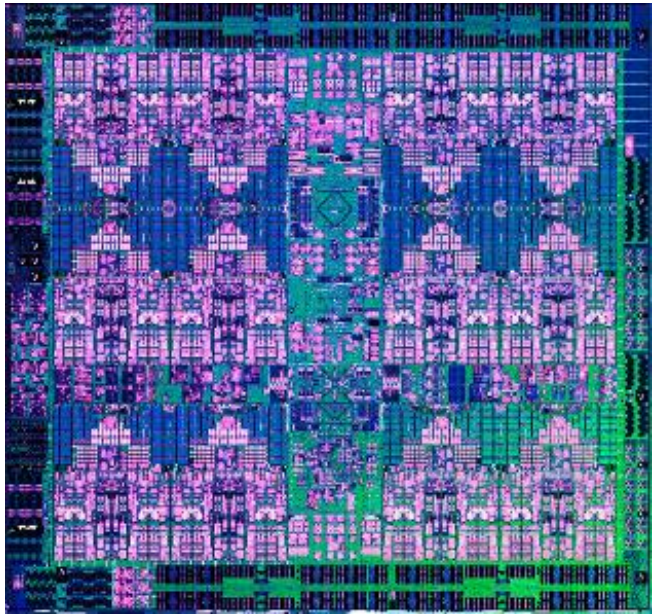
Performance and Scaling

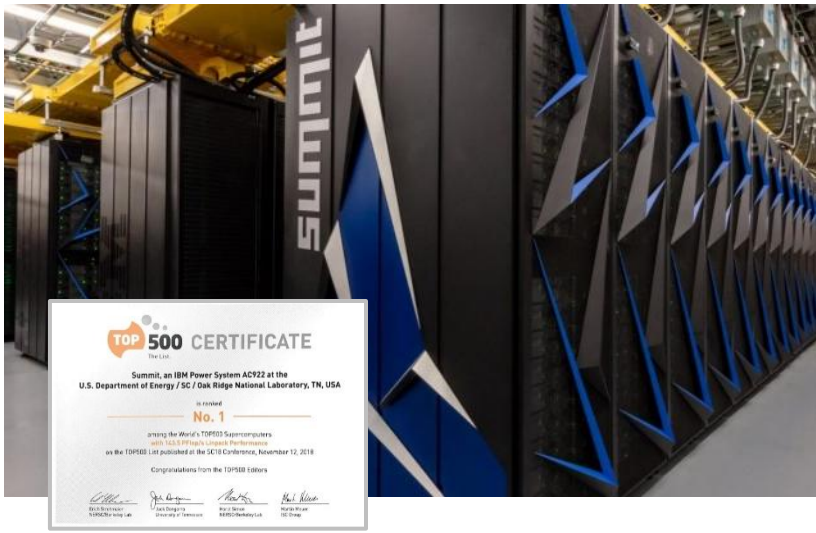
- Strong Thread x SMT8
- 16-wide execution, Deeply Out-of-order pipeline
- Huge 128M L4
- Up to 12 cores per socket
- Large System Scaling Boost

Open Innovation

- CAPI attach
- Centaur Memory
- PCI I/O attach
- OpenPOWER

POWER9 (2018)

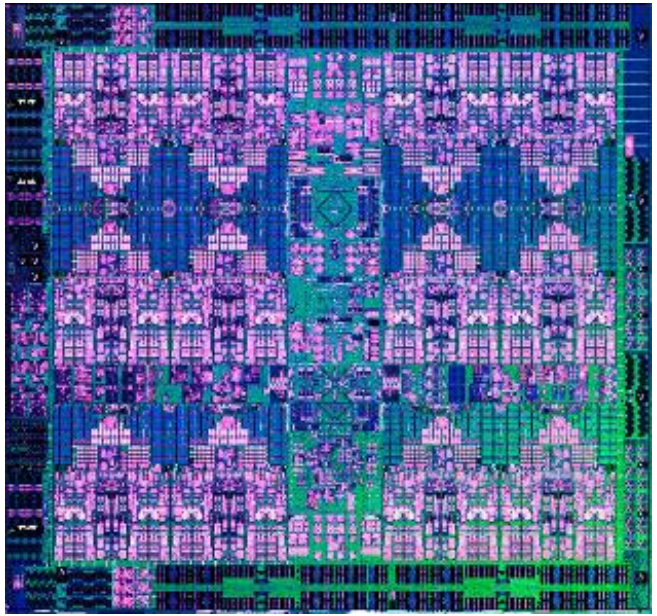


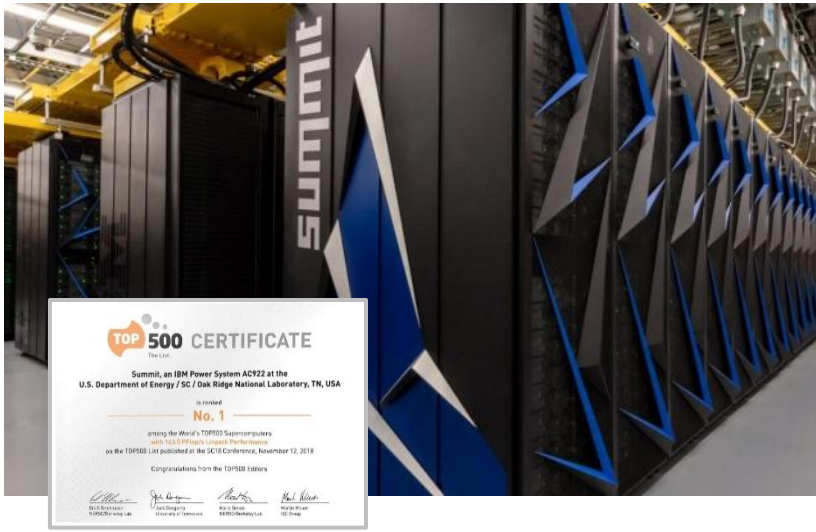


Objectives

- Core Strength
- Modular Core Architecture to span Enterprise and OpenPower
- Multiple Memory Architectures (Centaur + Direct Attach)
- Enterprise System Scaling
- Massive, Robust Data Plane
- Accelerated Computing / AI Training → Supercomputer Focus

POWER9 (2018)



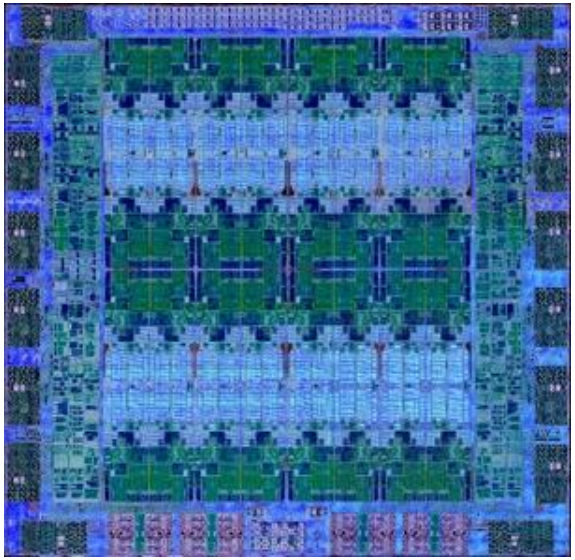


Enterprise

- Modular SMC Core Strength
- Large Robust Cache Architecture
- 2x Bandwidth Coherence & Data Plane
- In-Memory DataBase Supremacy
- Large System Resurgence

Supercomputer / Accelerated

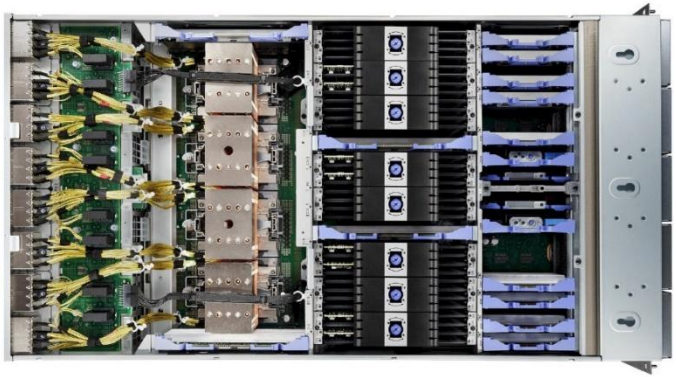
- #1 and #2 Supercomputers on earth
- NVLINK Coherent GPU Attach
- Direct Memory Attach Architecture
- PowerAXON Composability
- Leadership clustered AI Training

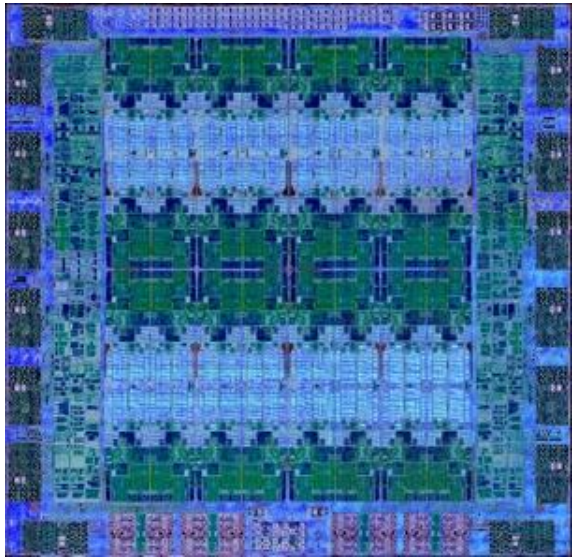


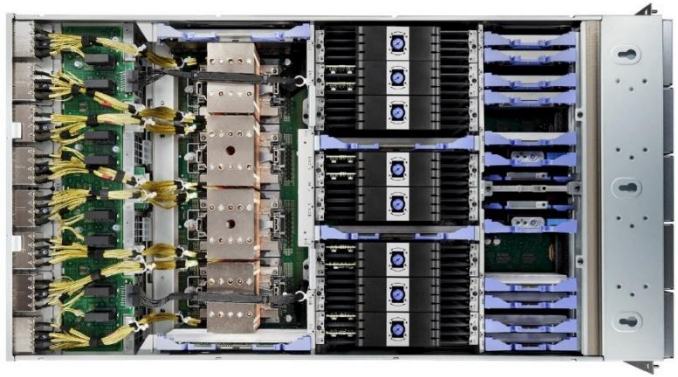
Power10 (2021)

Objectives

- Stronger enterprise core and thread
- Massive single socket performance boost
- Extreme in-core AI capabilities focused on inference
- Energy efficiency → sustainability
- Data plane bandwidth, capacity, composability, scale
- Hardware assisted security capabilities







Power10 (2021)

Computational Capability

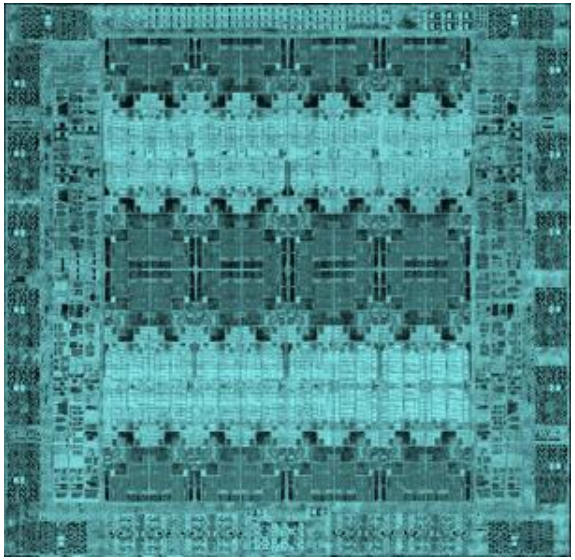
- Powerful new core architecture
- 20% thread speed, 30% core strength
- DCM enables >2x socket performance
- Massive AI infusion: up to 20x per socket
- Energy efficiency improvement: >2x

Security

- 4x crypto engines per core
- Transparent main memory encryption
- Transparent side-channel evasion

Data Plane Scale and Composability

- New OMI memory architecture
- PCIe G5 and up to 64 lanes per socket
- Memory Clustering

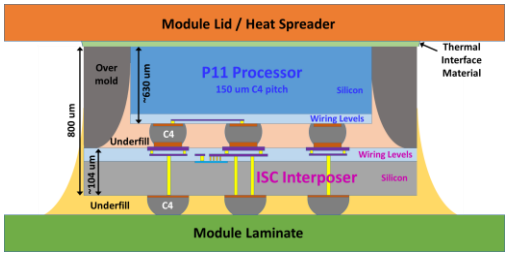


Power11 (2025)

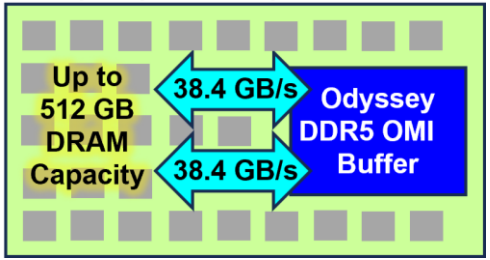
Objectives

- Improve Core and Thread Strength
- Improve System Throughput for Entry & Midrange
- Enterprise AI inference and Fine-Tuning
- Improve Memory Architecture
- Fully Leverage Robust Power10 Architecture
- Focus on Stack Level Functionality

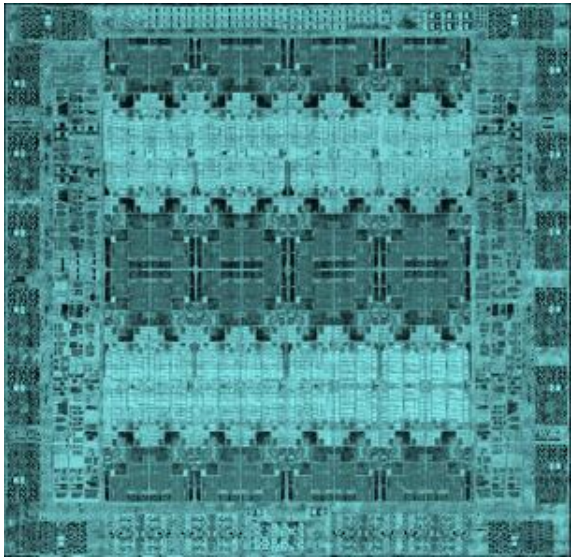
2.5D ISC Architecture



Odyssey DDR5 D-DIMM



Spyre AI Accelerator



Power11 (2025)

Computational Capability:

- 4.15 GHz growth to 4.4 GHz
- 50% Throughput growth for S1122

AI:

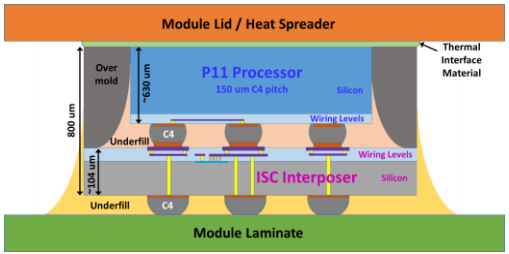
- MMA growth
- Accelerated Spyre

Stack Value:

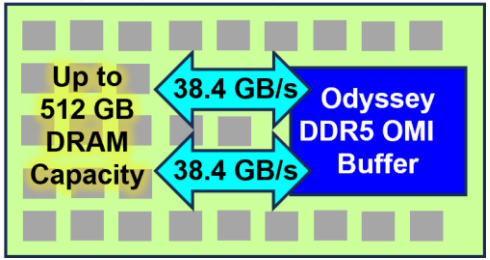
- Zero Planned Downtime
- Resource Groups
- Cyber-Resiliency

DDR5 OMI Memory: 3x Bandwidth!!!

2.5D ISC Architecture

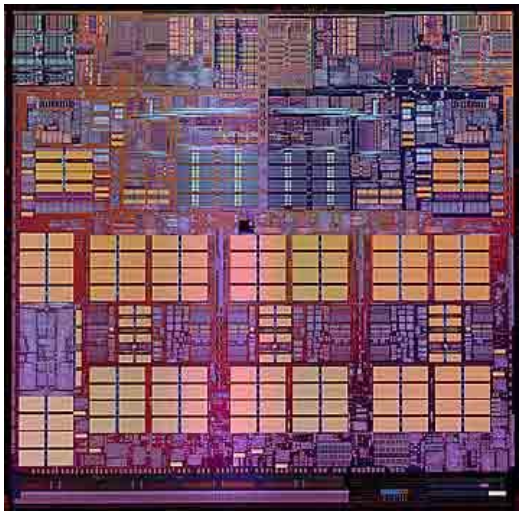


Odyssey DDR5 D-DIMM



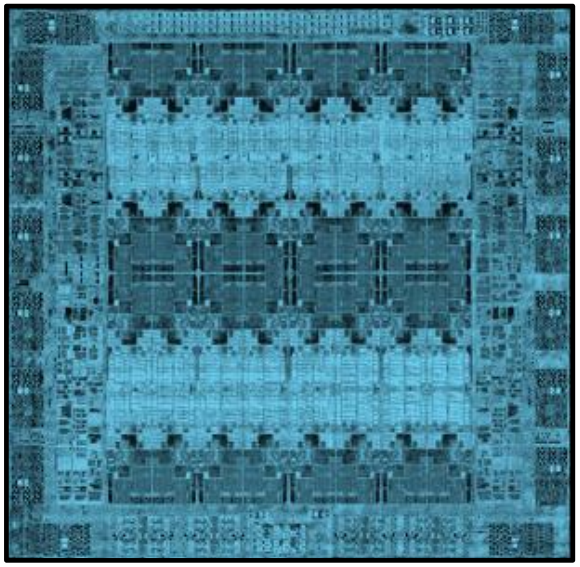
Spyre AI Accelerator

Massive Growth over 25 Years



POWER4 chip (2001)

168x Capacity Growth!



Power11 chip (2025)

Power 890 Max System
16 processor chips
CPW = 37,400

Power E1180 Max System
16 processor chips
CPW = 6,291,200

Looking Forward: The Enduring Strength of IBM i

- Forged from an Extreme Vision for Computing

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- Good Fortune or Brilliant Foresight?
- Ideal Platform to Meet Future Trends Head-on

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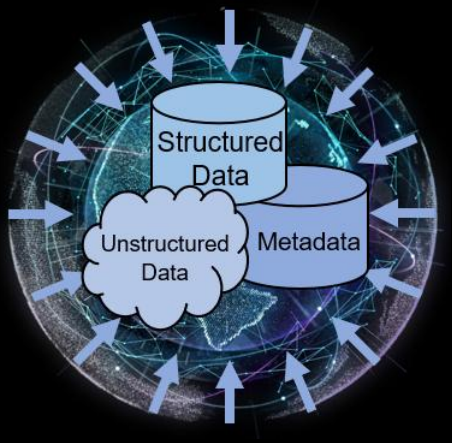

Societal Digitalization Drives Data Gravity

Database
Built into the Platform

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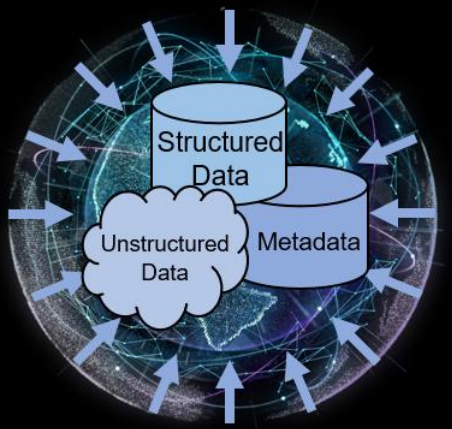

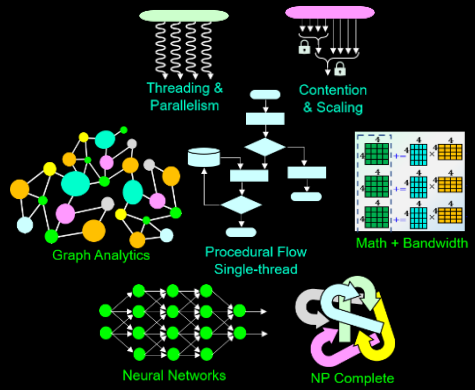

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Semiconductor Physics Drives Diverse Compute Paradigms

Inherent Object-Orientation & Hybrid Compute Optimization

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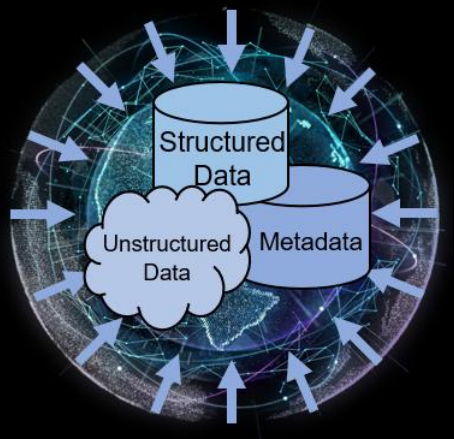

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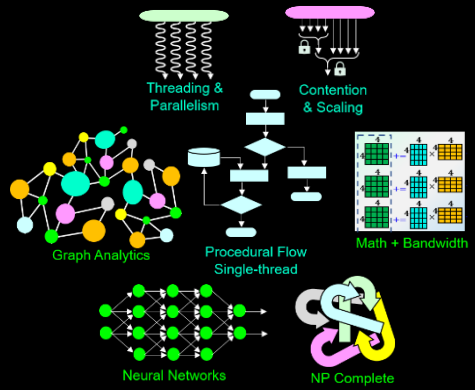
Database Built into the Platform



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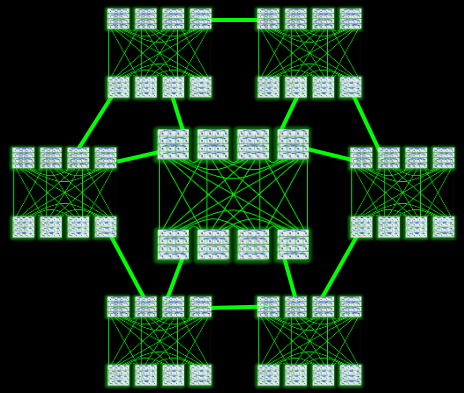
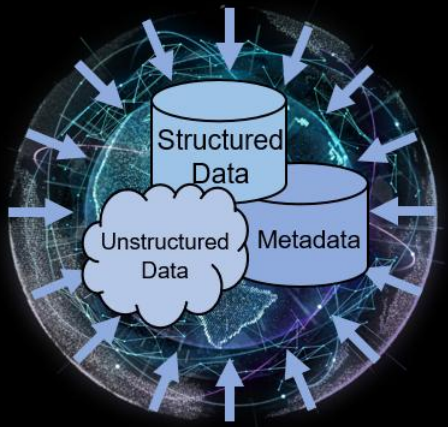


Data Gravity Drives Massive Resource Aggregation

Single-Level Store Architecture: Huge Name Space

Looking Forward: The Enduring Strength of IBM i

Thank You!



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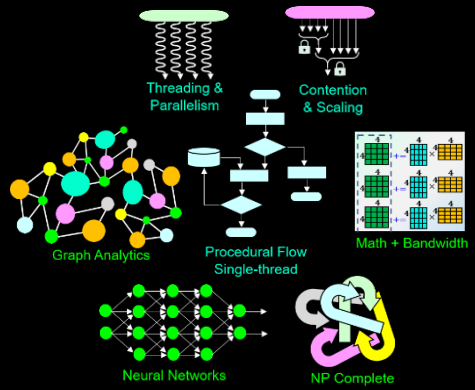

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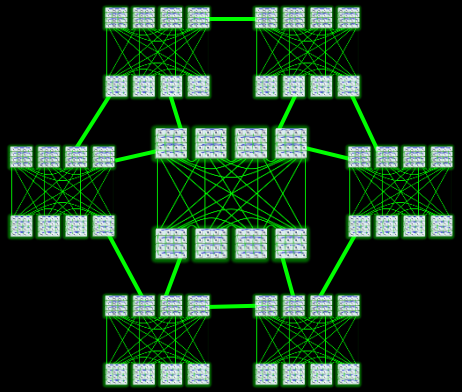

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