DPDK SUMMIT
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Low-Latency Sensor Bridge Solution for Perception Physical AI (Using DPDK)

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The latency bottleneck of Sensor-to-AI Inference

What Physical AI actually needs

- Real-time control loops, not batch throughput
- **Deterministic** sensor-to-AI latency (low jitter, bounded tail latency)

Where latency really accumulates

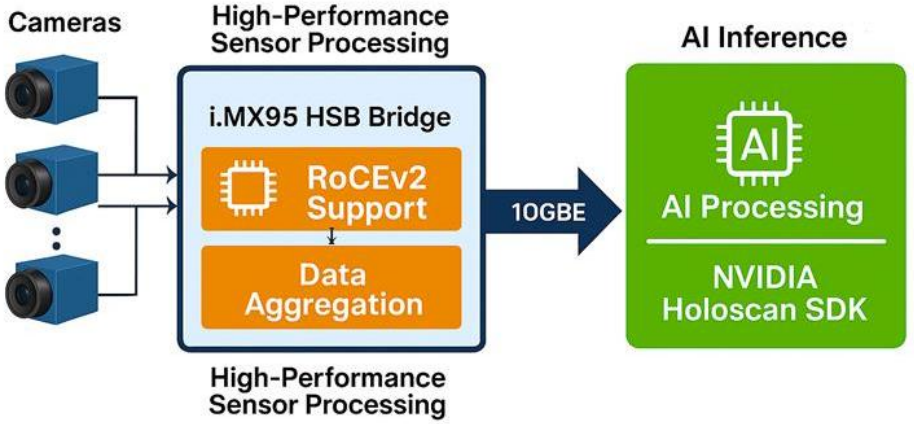
- Distributed sensors → centralized AI compute
- Sensor → CPU → kernel → network → user pipelines
- Multiple copies, buffering, interrupts, and scheduler noise

Why inference optimizations alone are not enough

- GPU inference latency may be milliseconds
- Sensor delivery jitter can exceed inference time
- Late or jittery sensor data breaks perception-control loops

DPDK Enabled Holoscan Sensor Bridge with Nvidia Physical AI Processing

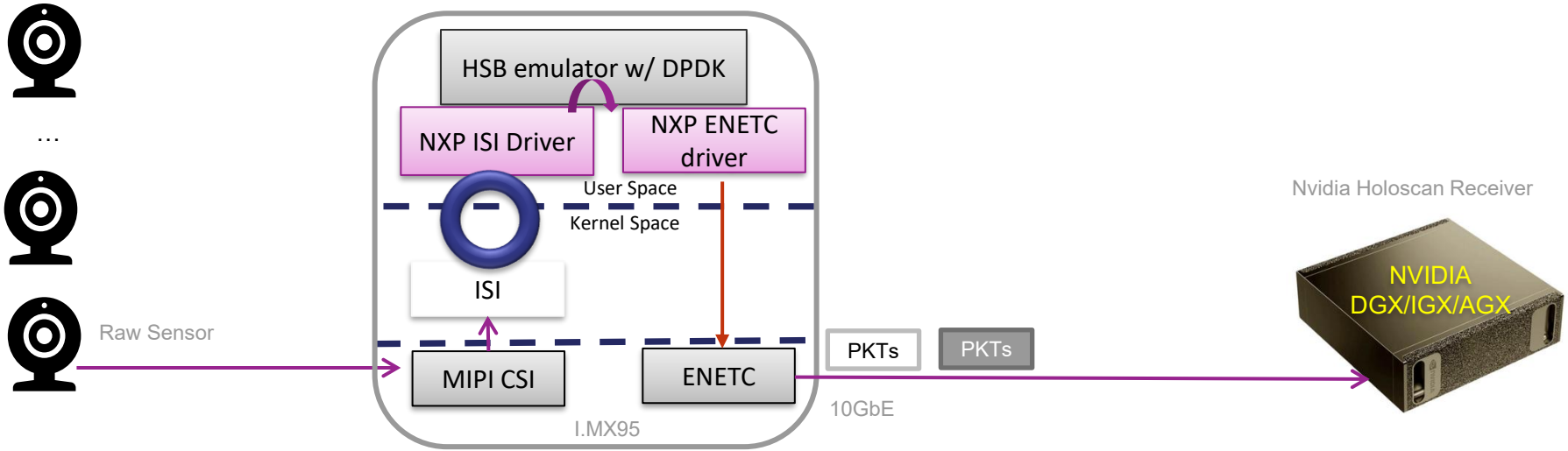
- NXP i.MX95 runs a DPDK-controlled userspace sensor dataplane as a Holoscan Sensor Bridge (HSB)
- Sensors act as first-class DPDK producers, not kernel-bound peripherals
- Zero-copy, poll-mode datapath for real-time sensor packetization at the edge
- Streams high-rate camera data (e.g., 4K@60) from i.MX → NVIDIA platforms
- Designed for deterministic latency, bounded jitter, and CPU-efficient transport



Not "AI on i.MX" — but DPDK-enabled, AI-ready sensor transport for:

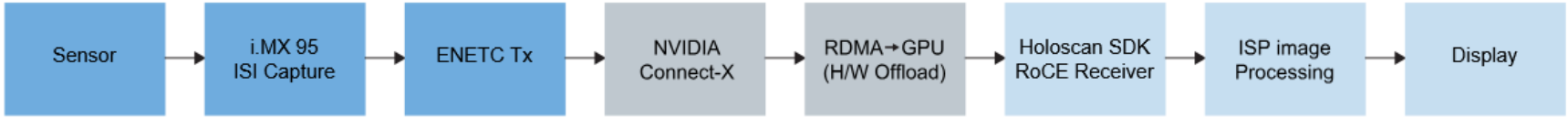
- Humanoid robotics
- Perception-driven machines
- Physical AI pipelines

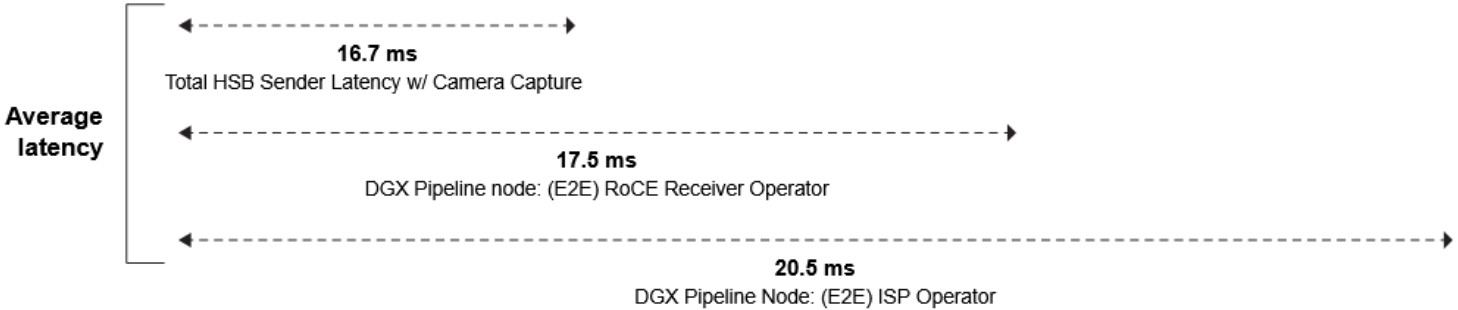
DPDK BASED HSB IMPLEMENTATION ON I.MX95



- DPDK-controlled userspace dataplane with full ENETC control (no kernel jitter)
- Zero-copy sensor-to-network path via DPDK ISI rawdev
- Line-based camera data → packets for deterministic, low-latency transport
- Scales from single-sensor to multi-sensor fusion
- Supports RDMA/RoCE, Linux sockets, and Camera-over-Ethernet

Latency Benchmarks with RoCEv2: 4K@60 FPS with NVIDIA DGX SPARK





	Avg Latency (ms)
Camera Capture (4K@60FPS)	15.6
Total HSB Sender Latency with Camera Capture(I.MX95)	**16.7**
DGX Pipeline Node : (E2E) RoCE receiver operator	**17.5**
DGX Pipeline Node : (E2E) ISP Operator	**20.5**

Summary & Outlook

- Key Takeaways
  - NXP demonstrates FPGA/ASIC-class sensor dataplanes on a general-purpose microprocessor
  - Achieved by leveraging DPDK's userspace, zero-copy, poll-mode execution model
  - Enables deterministic, low-latency sensor-to-AI transport over standard Ethernet
  - Expands DPDK's relevance into robotics, industrial vision, and Physical AI

- What's Next
  - Multi-sensor time synchronization and fusion-ready pipelines
  - DPDK + TSN integration for time-aware, bounded-latency transport
  - Reusable sensor-to-AI transport patterns for the DPDK ecosystem

Related Ecosystem & Platforms

https://www.nxp.com/applications/technologies/ai-and-machine-learning/humanoid-robotics-and-physical-ai:PHYSICAL-AI

https://www.nvidia.com/en-us/technologies/holoscan-sensor-bridge/?deeplink=partners-tab--2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