



Verifying all the flexibility of RISC-V within SoC DV test plans

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Agenda

- RISC-V verification issues
- Compliance is not verification
- Reference models and custom instructions
- Processor IP verification
- SoC level verification
- Summary

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RISC-V Presents New Challenges



- RISC-V is a new ISA – an open standard ISA
 - Managed by the non-profit RISC-V International (www.riscv.org)
 - This means any designer can build a processor implementation
 - (today (mid 2020) there are almost 100 RTL designs including open source and proprietary)
- Traditionally, processor IP ...
 - comes from, and is maintained by, the ISA owner
 - is single sourced
 - comes fully verified and compliant to that specific ISA
- All users need to do is to verify using integration tests
- There is no “standard” approach and there are few available tools for processor verification
- The RISC-V industry / ecosystem needs to adapt best practices for SoC verification to processor verification

To be more specific about the RISC-V DV Problem



- Arm processor IP
 - $\sim 10^{15}$ verification cycles per processor
 - Verification of interface between NoC and processor
 - 1,000s of SoC designs successfully produced
- Similar approaches for ARC, MIPS, Tensilica, ...
- RISC-V IP
 - How well verified is an individual processor (from processor IP vendor, open source, self-built)?
 - How to verify processor subsystems, especially for AI/ML architectures?
 - How well verified is interface between NoC and processor?
 - How to deal with custom instructions?

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Compliance Testing



- The device works within the envelope of the agreed specifications
 - “Have you read and understood the specification”
- Testing of the instructions should
 - Attempt to use all registers as source and destination (not combinations)
 - Attempt to operate on all bits which compose the immediate values (1 / 0)
 - Capture a signature in memory region indicating the test result
 - Based upon a particular hardware configuration
 - Compare the signature against a known good reference
 - Static (pre defined signature extraction)
 - Dynamic (runtime generation from YAML configured reference)

Compliance Testing (2)

- Testing of the instructions does NOT
 - Attempt to stress all possible aspects of functional verification, e.g.:
 - All possible combinations of instruction parameters (2-in, 1-out = 32,768)
 - All possible data values
 - Attempt to expose possible micro-architectural aspects
 - Attempt to exercise behavior which generates an exception
 - Illegal instructions (unsupported extensions)
 - For example, do not test for missing M instructions in context of RV32I
 - Illegal conditions (misaligned fetch, load, store)

These tasks all come under the Design Verification (DV) heading

Compliance Testing (3)

- Test Qualification – assess how good/effective the tests are
 - Functional Coverage analysis
 - Mutation Fault Simulation - Testing analysis (Imperas work in progress)
 - Provides Decode Coverage
 - Sees if observe changes on all bits of legal decodes

Compliance Testing (4)

- Test Qualification
 - Functional Coverage analysis
 - Mutation Fault Simulation - Testing analysis (Imperas work in progress)
 - Provides Decode Coverage
 - Sees if observe changes on all bits of legal decodes
 - Verified against RV32I test suite
 - 48 hand coded directed tests (average 150 instructions each)
 - <https://github.com/riscv/riscv-compliance/tree/master/riscv-test-suite/rv32i/src>

Compliance Testing (5)

- Compliance RV32I Base Instruction Testing
 - (Nov 2019) 48 tests, 97% functional 'basic' coverage, ~35% 'extended' coverage
- Imperas RV32/64V vector instruction Compliance Test Suite
 - 90 different vector engine configurations x ~500 vector instructions
 - (Aug 2020) 1,500-7,000 tests (depends on vector engine configuration)
- RISC-V International's compliance suites are still a work in progress

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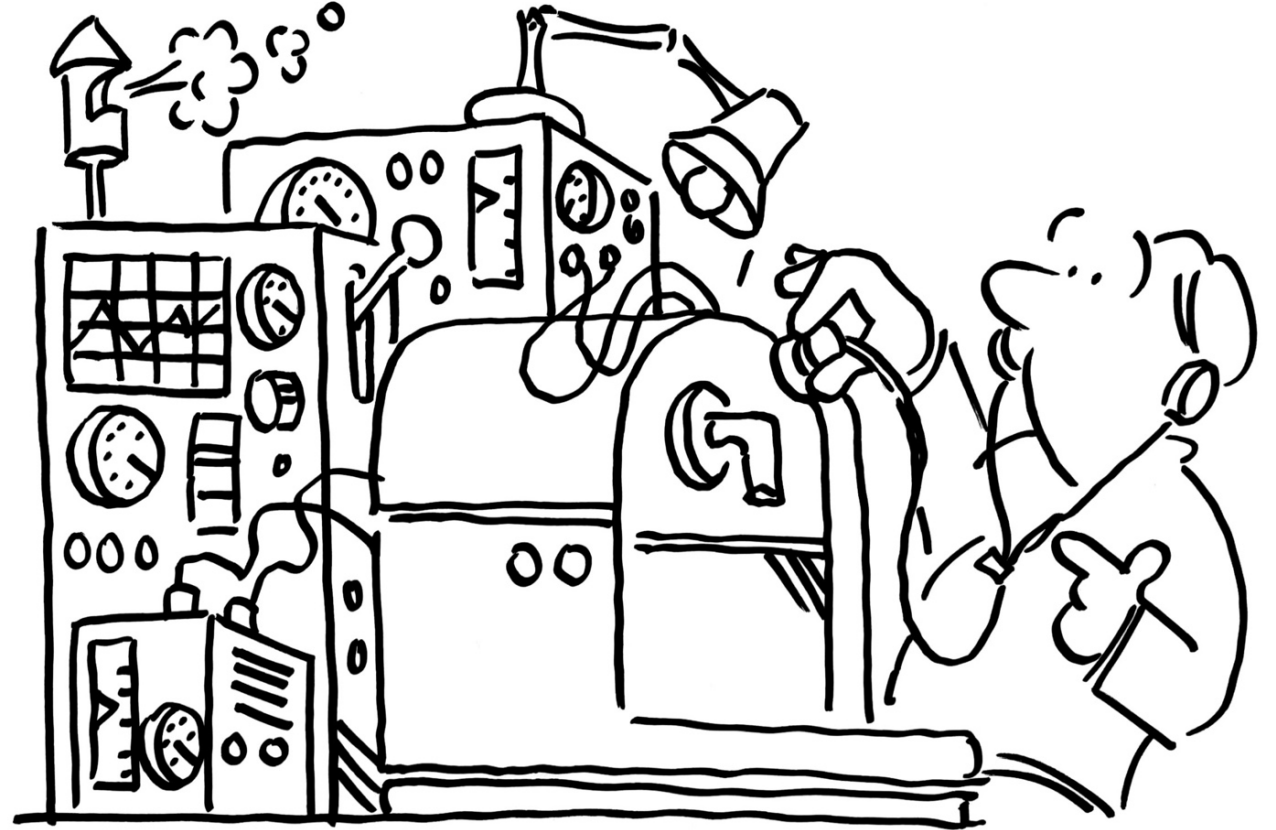
Key Issue – Reference Comparison



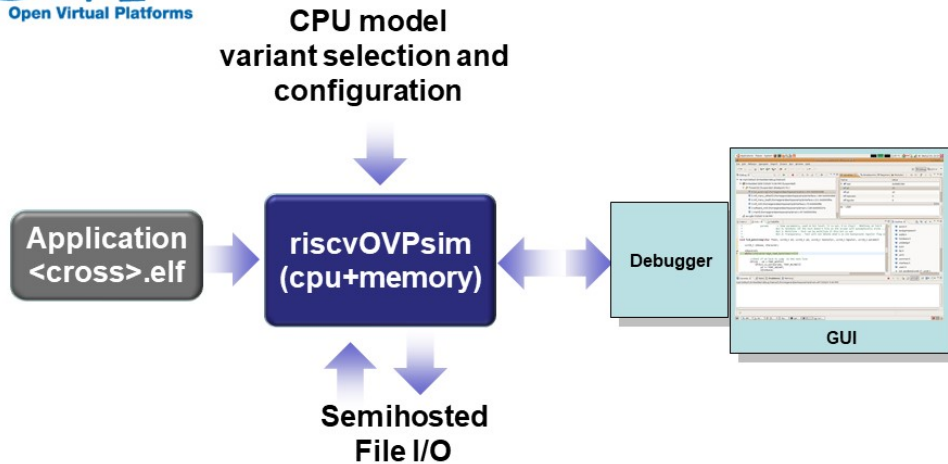
- One thing compliance, directed, random have in common...
 - Is a need for a reference implementation to compare with
- So why is there a need for a reference as part of hardware design verification ?
 - Comparison for the observed behavior
 - Covering all possible aspects of the ISA envelope
- And – it needs to represent the exact design and architecture being tested, for example:
 - XLEN
 - Vectors: VLEN, SLEN, ELEN, (version: 0.8, 0.9, 1.0, ...)
 - Bit Manipulation (version: 0.91, 0.92, 1.0)
 - Custom Extensions
 - M+U (No S)
 - Hardware LSU Misalignment Support (no exceptions)
 - CSR: MTVEC Read Only
 - ...

RISC-V Reference Choices

- RISC-V is highly configurable
- So it can get a little complicated
- 60 Questions ?



riscvOVPsim as the Reference Model for Compliance Testing



Imperas riscvOVPsim Compliance Simulator

- Industrial quality, free ISS / reference model for compliance testing
 - <https://github.com/riscv/riscv-compliance>
 - <https://github.com/riscv/riscv-bitmanip>
- Model is built using Open Virtual Platforms (OVP) APIs
- Implements full RISC-V envelope
 - Configurable for all features and versions
- Includes full open source Apache 2.0 model
- Kept up to date for specification changes
- Works 'out of the box' with full tracing, debug, and many other options
- Video: <https://www.imperas.com/riscvovpsim-complete-risc-v-iss-bare-metal-software-development-and-specification-compliance-test>
- Has some limitations which make it not appropriate as a reference model for RTL design verification (DV)
 - Imperas have other simulators/models for those tasks

Additional Capabilities Needed for a DV Reference Model



- Support for multi-hart processors and concurrency
- Support for custom instructions
- Support for injection of external / asynchronous events
 - Including control of external interrupts controllers
- Support for control of Debug Mode interactions
- Support for step-and-compare DV flow
 - With reference model encapsulated in SystemVerilog testbench

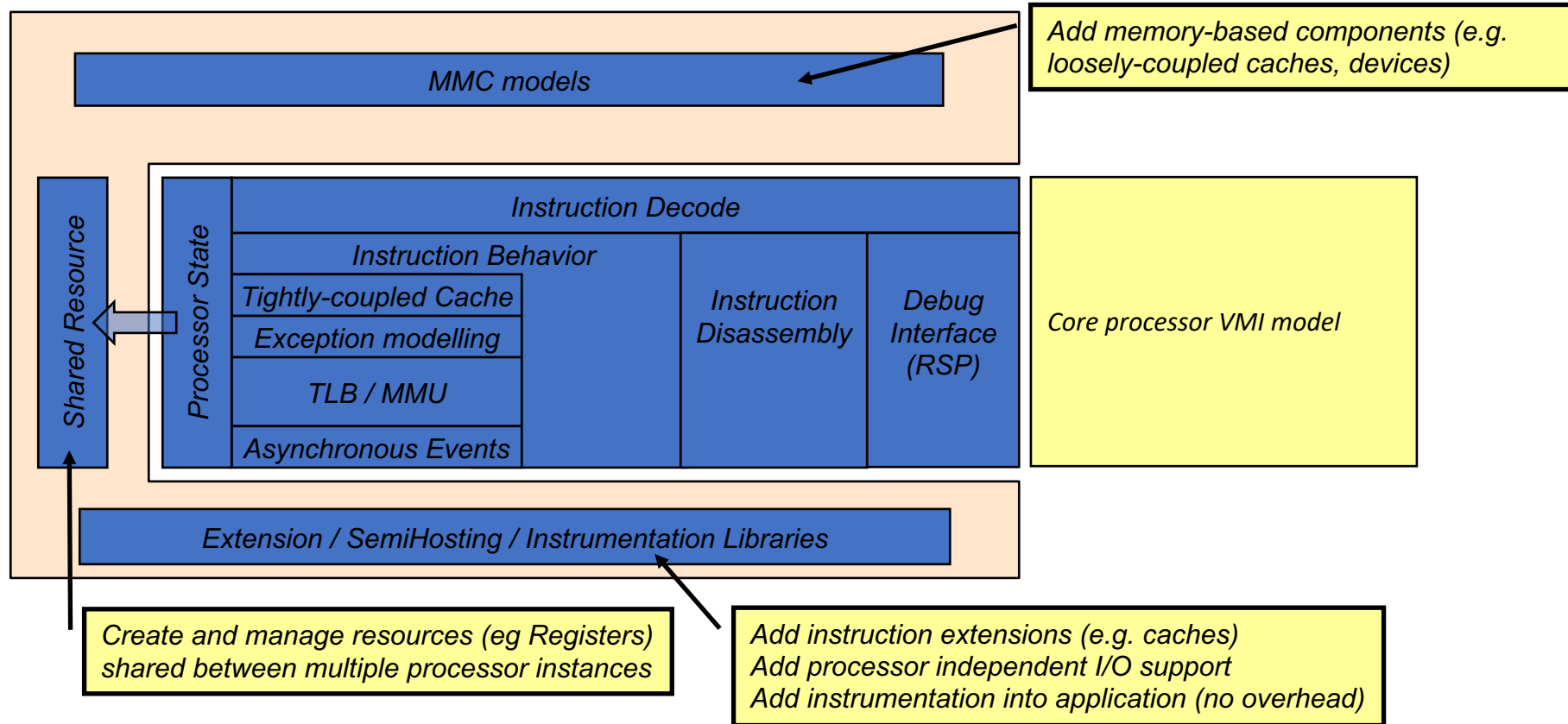
OVP RISC-V Model and Imperas Simulator as Reference



<http://www.imperas.com/riscv>

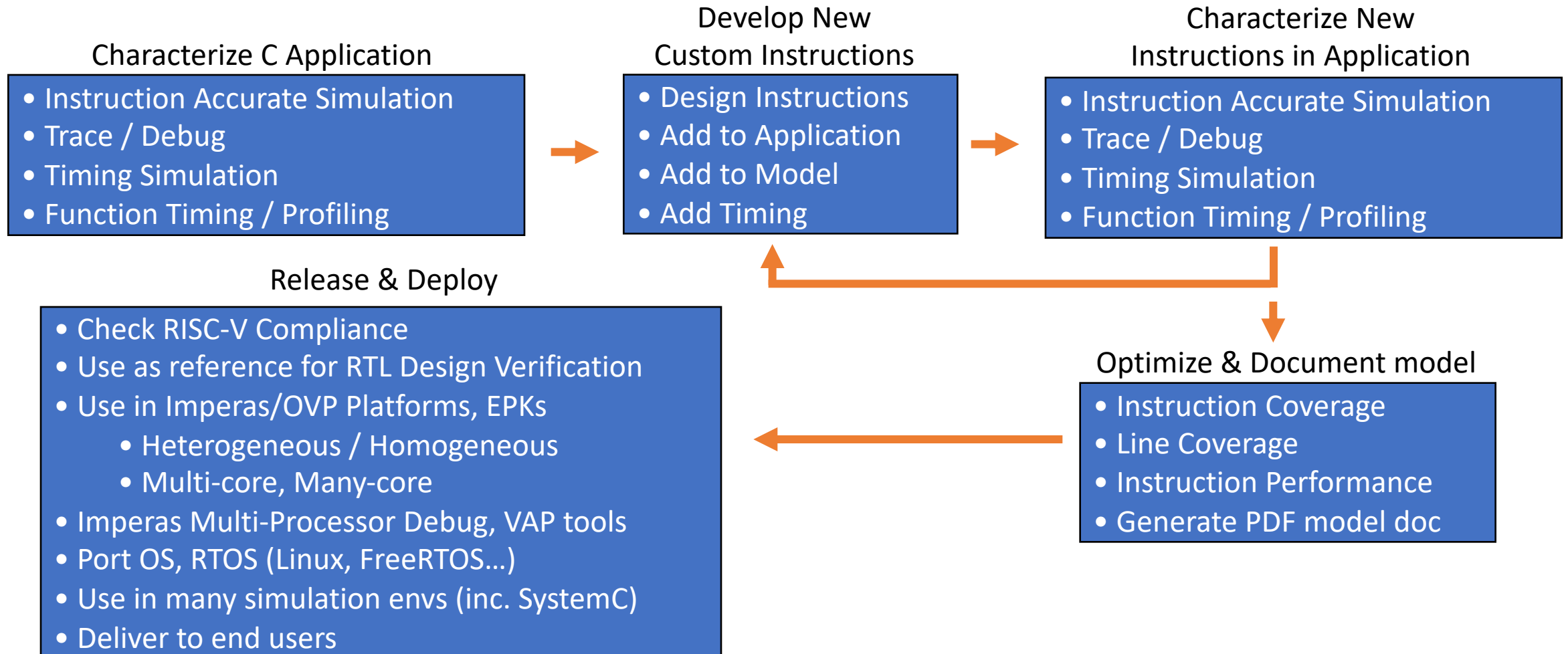
- Support for multi-hart processors
- Support for custom instructions
- Support for injection of external / asynchronous events
- Support for step-and-compare DV flow
- Used as golden reference in RISC-V Foundations' Compliance Suite and Bit Manipulation group
- In use as reference with customers for RTL DV
 - Public announcements include
 - Mellanox Technologies
 - OpenHW Verification Task Group
 - Google open source ISG project
 - RISC-V International Compliance Working Group

Imperas Processor Models Components



=> complete proven technology, methodology, with development tools – 12 public ISAs, 7 proprietary ISAs, 300+ models

Flow to add new custom instructions



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- RISC-V verification issues
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- **Processor IP verification**
 - **Step and compare methodology**
 - **Directed tests**
 - **Instruction stream generation**
 - **Test generation and execution**
- SoC level verification
- Summary

Two choices for Directed Testing: self check vs reference compare



- Test Encoded Self Checking
 - Tests are written with expected behaviour encoded
 - Tests can introspect the state and (self) diagnose faults
- Reference Comparison Checking
 - Tests are written without predicting the result
 - A reference is consulted for the correct value

```
// Device Under Test  
int a = 4; int b = 5;  
int c = a + b;  
// c == ?
```

```
// Reference  
int Ra = 4; int Rb = 5;  
int Rc = Ra + Rb;  
// Rc == 9
```

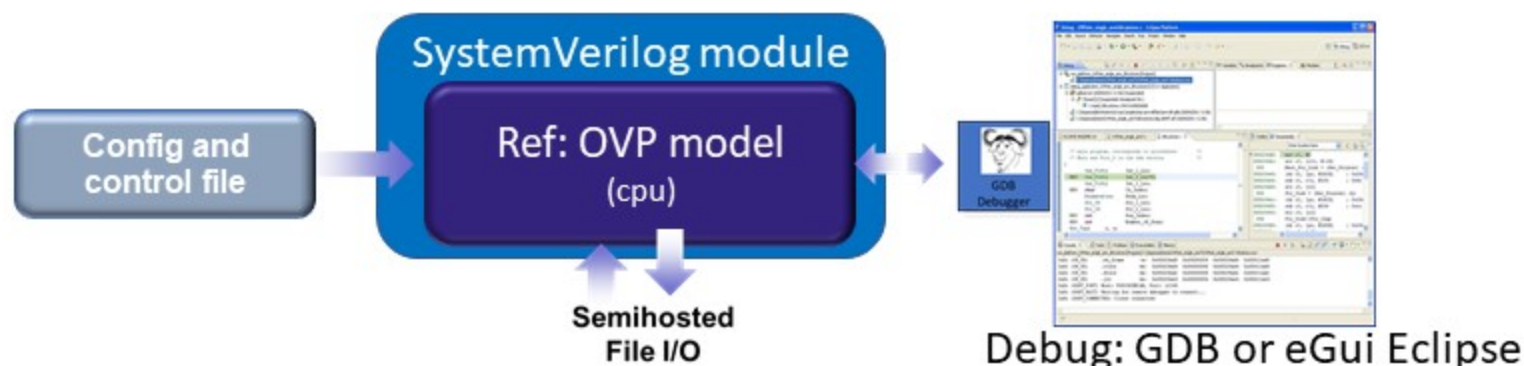
```
assert(c == Rc) // external (@runtime or post-processed)
```

Two choices for compare DV Methodology: Post process Trace/Signature Compare vs Step and Compare



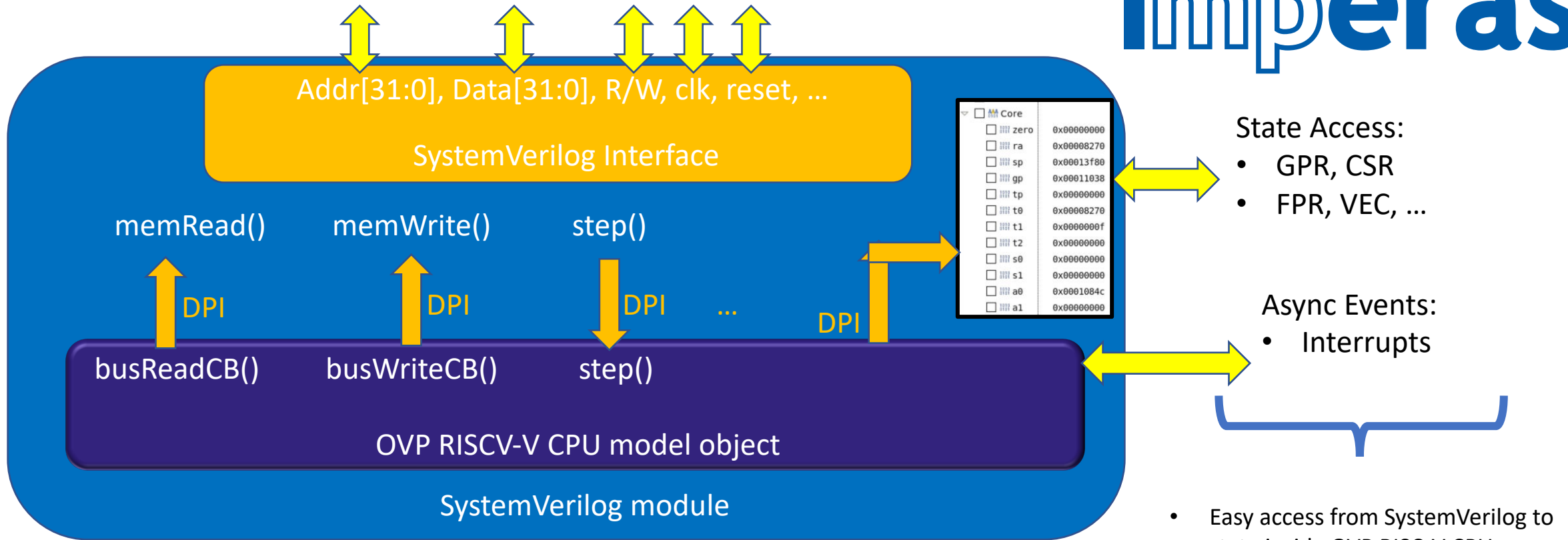
- Short answer: bottom line is DV resources used
 - DV is already taking 70% of the design resources, so efficiency of these resources is critical
- With post process comparison (trace or signature)
 - Failures are not known until after the simulation has completed
 - this can be a long time for a complex test
 - Errors might get programs into e.g. loop conditions
 - Binary result – not shows where the instruction/state change is that diverged
 - Often waste significant simulation and staff resources to diagnose/track down
- Step and compare enables failures to be flagged and the simulation stopped when the failure occurs

OVP model in SystemVerilog



- OVP model is encapsulated into a SystemVerilog module
- A model of RISC-V Foundation's standard ISA and ISA extensions (RV32/64 IMAFDC + B + V)
 - Includes variants for all standard configurations
- Single processor instantiation with Memory etc all in SystemVerilog
- Interfaces: reset, step, address bus, data bus, interrupts, etc.
- Like riscvOVPsim it has full trace and logging capabilities
- Does work with a side-port for GDB or Eclipse eGui debug or Imperas Multi Processor debugger (eGui MPD)
- And – users can extend it with custom instructions, state etc, ...

Imperas OVP Model Encapsulation

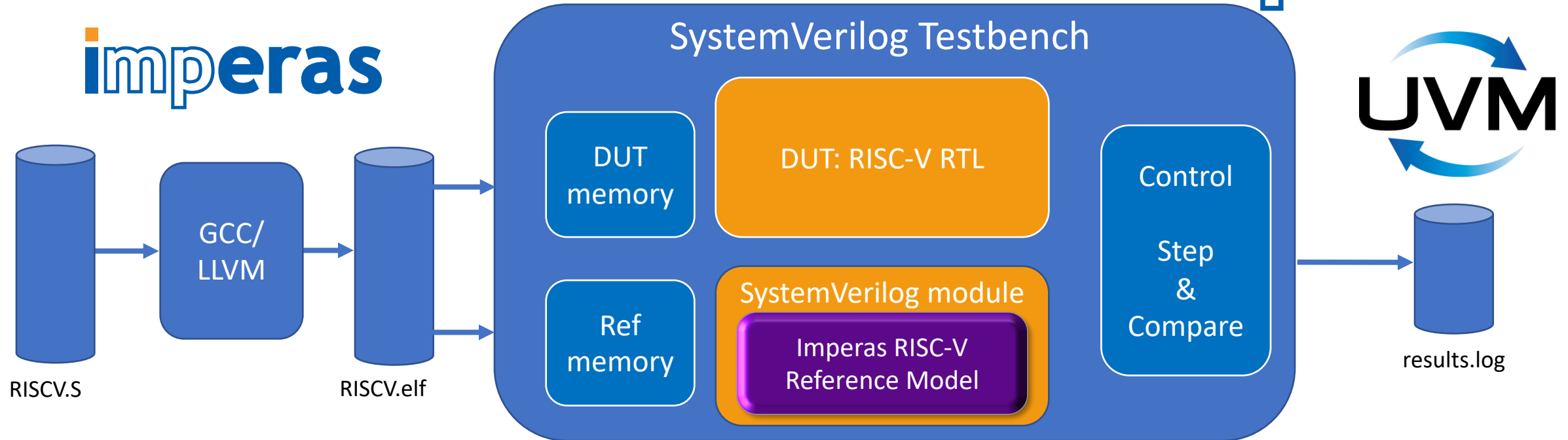


- OVP model is a binary shared object of a RISC-V CPU model
- Encapsulated into a SystemVerilog module, using SystemVerilog DPI
- Instanced in SystemVerilog design or testbench like any module
- Control interface so SystemVerilog can load programs, reset, clock, stop, start, ...
- Access to OVP model state registers and events from SystemVerilog

- Easy access from SystemVerilog to state inside OVP RISC-V CPU model
- Easy to trigger events from SystemVerilog into OVP model

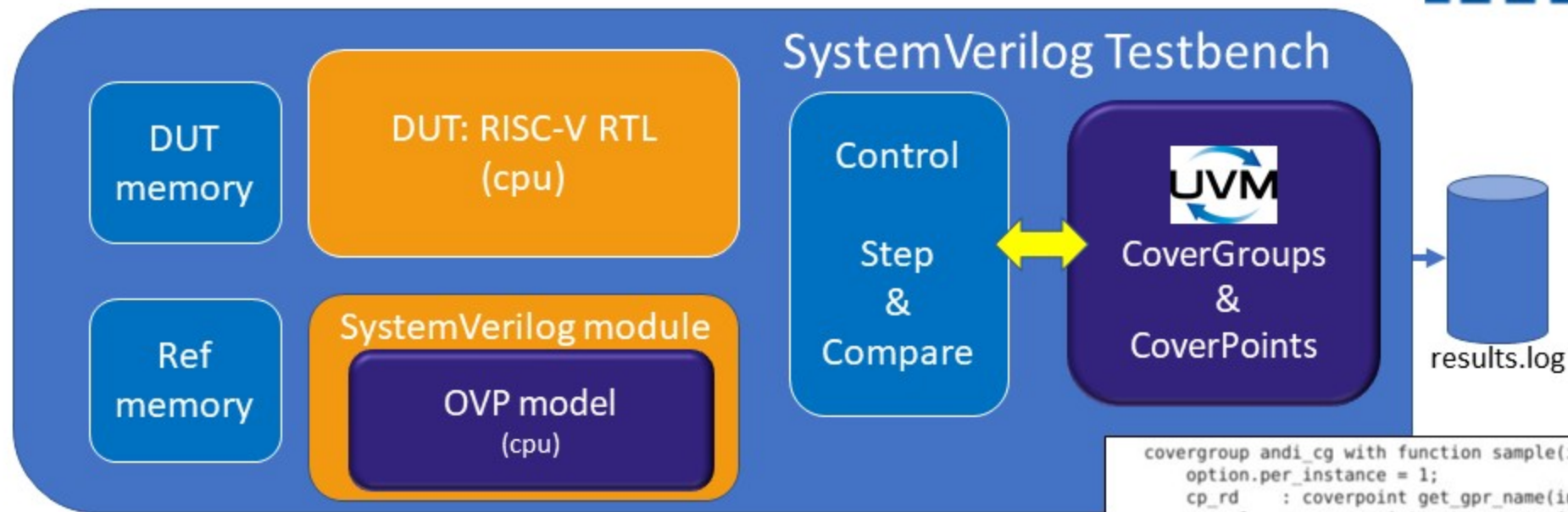
Step and Compare Flow

imperas



- Testbench loads .elf program into both memories, resets CPUs (RTL and OVP model)
- Steps CPUs (DUT and reference), extracting data, and comparing
 - There is no stored log file – test log data is dynamic and requires two targets to be run and compared

SystemVerilog Functional Coverage



- Testbench has class of CoverGroup and CoverPoints for each instruction
- CPU functional coverage sampled on 'retire instruction' event
- Coverage directly from simulation as part of testbench, not through post process of log files

```
covergroup andi_cg with function sample(ins_t ins);
    option.per_instance = 1;
    cp_rd    : coverpoint get_gpr_name(ins.ops[0].val, ins.ops[0].key, "andi");
    cp_rs1   : coverpoint get_gpr_name(ins.ops[1].val, ins.ops[1].key, "andi");
    cp_imm11  : coverpoint get_imm(ins.ops[2].val, "andi") {
        bins neg = {[0:-1]};
        bins zero = {0};
        bins pos = {[1:$]};
    }
endgroup
```

SCORE	INSTANCES	WEIGHT	GOAL	AT LEAST	PER	INSTANCE	AUTO	BIN	MAX	PRINT	MISSING
46.88	46.88	1	100	1	1		64		64		
CATEGORY	EXPECTED	UNCOVERED	COVERED	PERCENT							
Variables	96	51	45	46.88							
VARIABLE	EXPECTED	UNCOVERED	COVERED	PERCENT	GOAL	WEIGHT	AT LEAST	AUTO	BIN	MAX	COMMENT
cp_rd	32	17	15	46.88	100	1	1	0			
cp_rs1	32	18	14	43.75	100	1	1	0			
cp_rs2	32	16	16	50.00	100	1	1	0			

Key Issue for Directed Testing: Functional Coverage



Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_coverage
/riscv_instr_pkg/riscv_instr_cover_group		76.24%						
TYPE add_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE sub_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE addi_cg	riscv_instr_co...	99.55%	100	99.55%		✓	auto(1)	
TYPE lui_cg	riscv_instr_co...	80.00%	100	80.00%		✓	auto(1)	
TYPE auipc_cg	riscv_instr_co...	80.00%	100	80.00%		✓	auto(1)	
TYPE sra_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE srli_cg	riscv_instr_co...	0.00%	100	0.00%		✗	auto(1)	
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE xor_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE or_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE andi_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE andi_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE beq_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE bne_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE blt_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE bge_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE bltu_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE bgeu_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE lb_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE lh_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
TYPE lw_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	

Name	Class Type	Coverage	Goal	% of Goal	Status	Included
/riscv_instr_pkg/riscv_instr_cover_group		76.24%				
TYPE add_cg	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rs1	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rs2	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rd	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rs1_sign	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rs2_sign	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_rd_sign	riscv_instr_co...	100.00%	100	100.00%		✓
CVP add_cg::cp_gpr_hazard	riscv_instr_co...	100.00%	100	100.00%		✓
CROSS add_cg::cp_sign_cross	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE sub_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE addi_cg	riscv_instr_co...	99.55%	100	99.55%		✓
TYPE lui_cg	riscv_instr_co...	80.00%	100	80.00%		✓
TYPE auipc_cg	riscv_instr_co...	80.00%	100	80.00%		✓
TYPE sra_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE srli_cg	riscv_instr_co...	0.00%	100	0.00%		✗
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE xor_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE or_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE andi_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE andi_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE beq_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE bne_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE blt_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE bge_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE bltu_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE bgeu_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE lb_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE lh_cg	riscv_instr_co...	100.00%	100	100.00%		✓
TYPE lw_cg	riscv_instr_co...	100.00%	100	100.00%		✓

Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_cove
/riscv_instr_pkg/riscv_instr_cover_group		76.24%						
TYPE add_cg	riscv_instr_co...	100.00%	100	100.00%		✓	auto(1)	
CVP add_cg::cp_rs1	riscv_instr_co...	100.00%	100	100.00%		✓		
CVP add_cg::cp_rs2	riscv_instr_co...	100.00%	100	100.00%		✓		
CVP add_cg::cp_rd	riscv_instr_co...	100.00%	100	100.00%		✓		
CVP add_cg::cp_rs1_sign	riscv_instr_co...	100.00%	100	100.00%		✓		
CVP add_cg::cp_rs2_sign	riscv_instr_co...	100.00%	100	100.00%		✓		
CVP add_cg::cp_rd_sign	riscv_instr_co...	100.00%	100	100.00%		✓		
bin auto[POSITIVE]		7176	1	100.00%		✓		
bin auto[NEGATIVE]		5158	1	100.00%		✓		
CVP add_cg::cp_gpr_hazard	riscv_instr_co...	100.00%	100	100.00%		✓		
bin auto[NO_HAZARD]		10832	1	100.00%		✓		
bin auto[RAW_HAZARD]		728	1	100.00%		✓		
bin auto[WAVEFORM]						✓		
bin auto[WAVEFORM]						✓		
CROSS add_cg								
bin <auto>PO						✓		
bin <auto>NE						✓		
bin <auto>PO						✓		
bin <auto>NE						✓		
bin <auto>PO						✓		
bin <auto>NE						✓		
TYPE sub_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE addi_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE lui_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE auipc_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE sra_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE slli_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
TYPE srli_cg	riscv_instr_co...	100.00%	100	100.00%		✓		
bin auto[ZERO]		329	1	100.00%		✓		
bin auto[RA]		313	1	100.00%		✓		
bin auto[SP]		315	1	100.00%		✓		
bin auto[GP]		407	1	100.00%		✓		
bin auto[TP]		453	1	100.00%		✓		
bin auto[T0]		345	1	100.00%		✓		
bin auto[T1]		389	1	100.00%		✓		
bin auto[T2]		423	1	100.00%		✓		
bin auto[S0]		403	1	100.00%		✓		
bin auto[S1]		409	1	100.00%		✓		
bin auto[A0]		483	1	100.00%		✓		
bin auto[A1]		352	1	100.00%		✓		
bin auto[A2]		377	1	100.00%		✓		
bin auto[A3]		396	1	100.00%		✓		
bin auto[A4]		352	1	100.00%		✓		
bin auto[A5]		412	1	100.00%		✓		
bin auto[A6]		358	1	100.00%		✓		
bin auto[A7]		387	1	100.00%		✓		
bin auto[S2]		429	1	100.00%		✓		
bin auto[S3]		382	1	100.00%		✓		
bin auto[S4]		368	1	100.00%		✓		
bin auto[S5]		348	1	100.00%		✓		
bin auto[S6]		442	1	100.00%		✓		
bin auto[S7]		323	1	100.00%		✓		
bin auto[S8]		399	1	100.00%		✓		
bin auto[S9]		414	1	100.00%		✓		
bin auto[S10]		382	1	100.00%		✓		
bin auto[S11]		448	1	100.00%		✓		
bin auto[S12]		415	1	100.00%		✓		
bin auto[S13]		415	1	100.00%		✓		
bin auto[S14]		354	1	100.00%		✓		
bin auto[S15]		312	1	100.00%		✓		
bin auto[S16]		100.00%	100	100.00%		✓		
bin auto[S17]		100.00%	100	100.00%		✓		

Automated instruction coverage reporting from Questa SystemVerilog functional coverage based on the Imperas RISC-V reference model

Coverage images from Mentor Questa SystemVerilog UVM Simulator

Instruction Stream Generation



- Instruction stream generation (ISG) generates random streams of instructions
- Generator given guidance to target specific instruction types and values
 - Many constraints required to get legal instruction sequences
- No predicted results, relies upon reference comparison
- This is just constrained random generation repurposed to processor DV
- Constrained random generation is a well-established part of SoC DV flows

Google RISC-V Instruction Stream Generation

- High quality SystemVerilog UVM DV infrastructure
- Open source (Apache 2.0)
- Drives a RISC-V core through corner cases and pushes it to the limit
- Requires reference and DUT to generate instruction trace disassembly
- Traces compared as post-process (neutral CSV format)
- Can compare values **and** program flow
 - dependant upon target capability
- Provides functional coverage for test quality, and to aid guidance

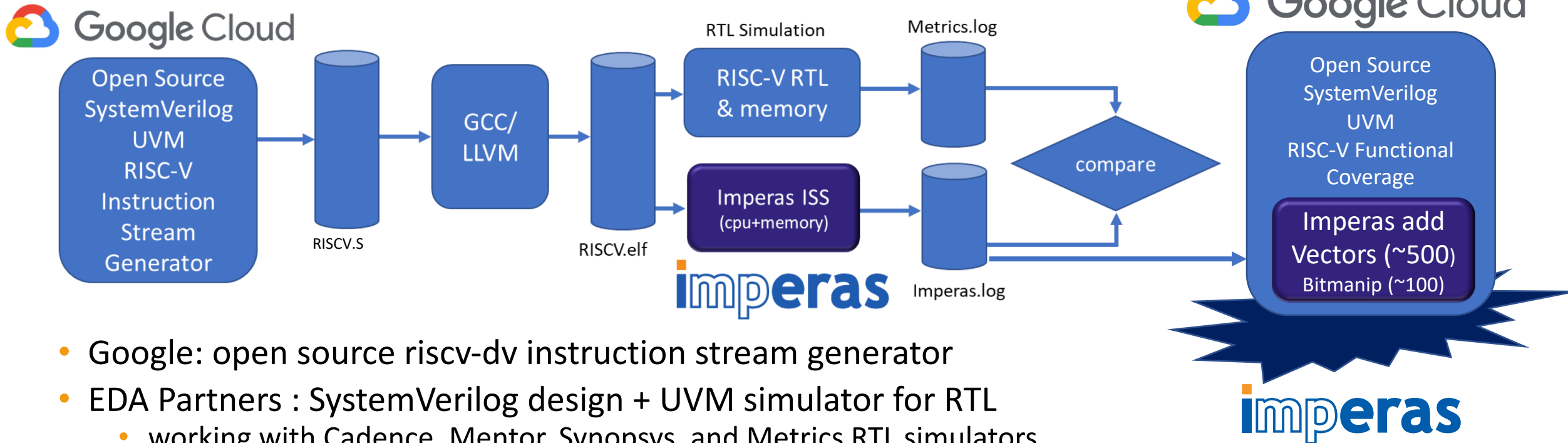


Open Source
SystemVerilog
UVM
RISC-V
Instruction
Stream
Generator

<https://github.com/google/riscv-dv>

Instruction Stream Generator Baseline Flow

imperas

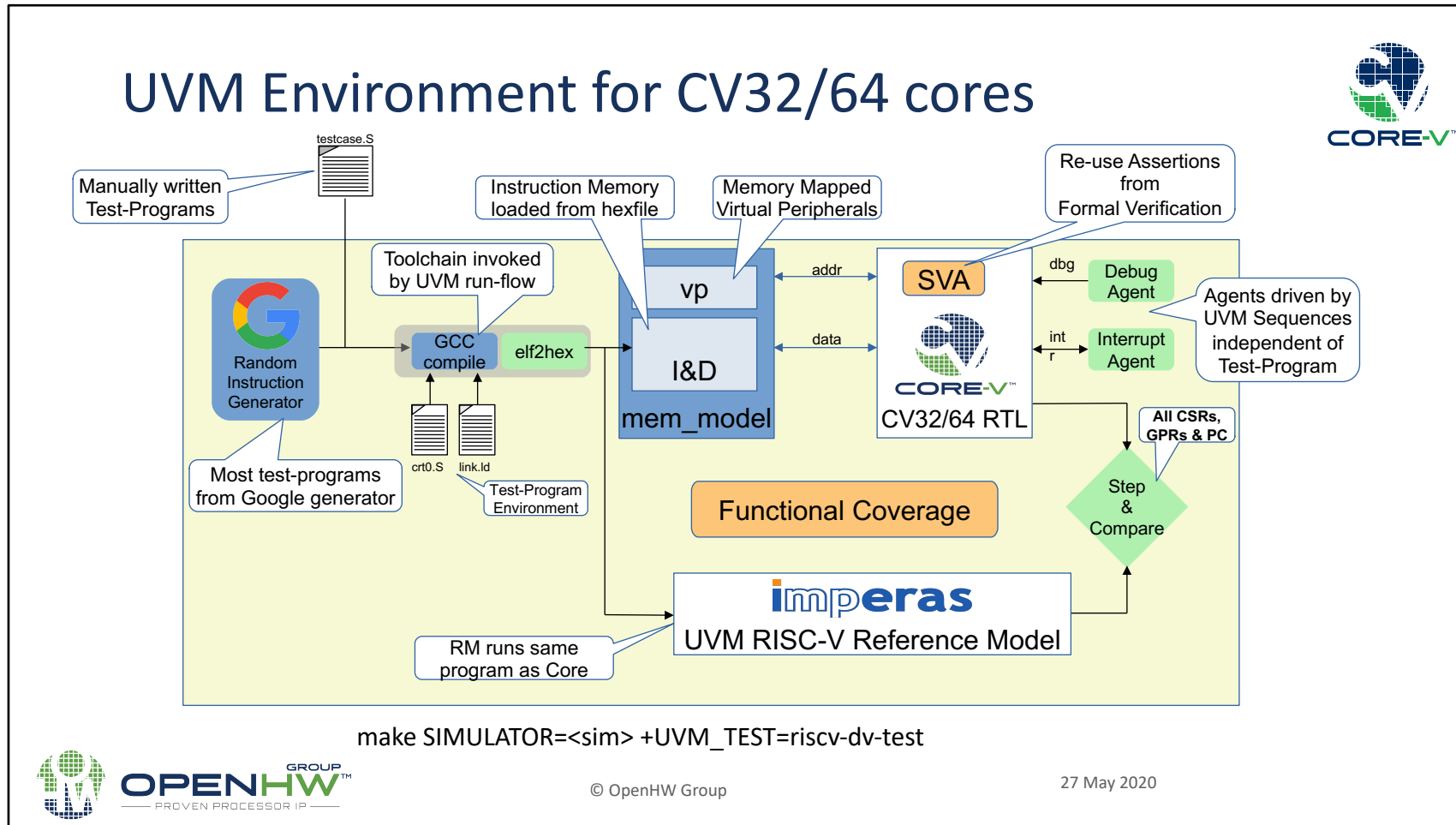


- Google: open source riscv-dv instruction stream generator
- EDA Partners : SystemVerilog design + UVM simulator for RTL
 - working with Cadence, Mentor, Synopsys, and Metrics RTL simulators
- Imperas: model and simulation golden reference of RISC-V CPU
- Imperas: extending this flow to support step-and-compare DV methodology

- Imperas have added Vector and Bitmanip extension instructions to the Functional Coverage

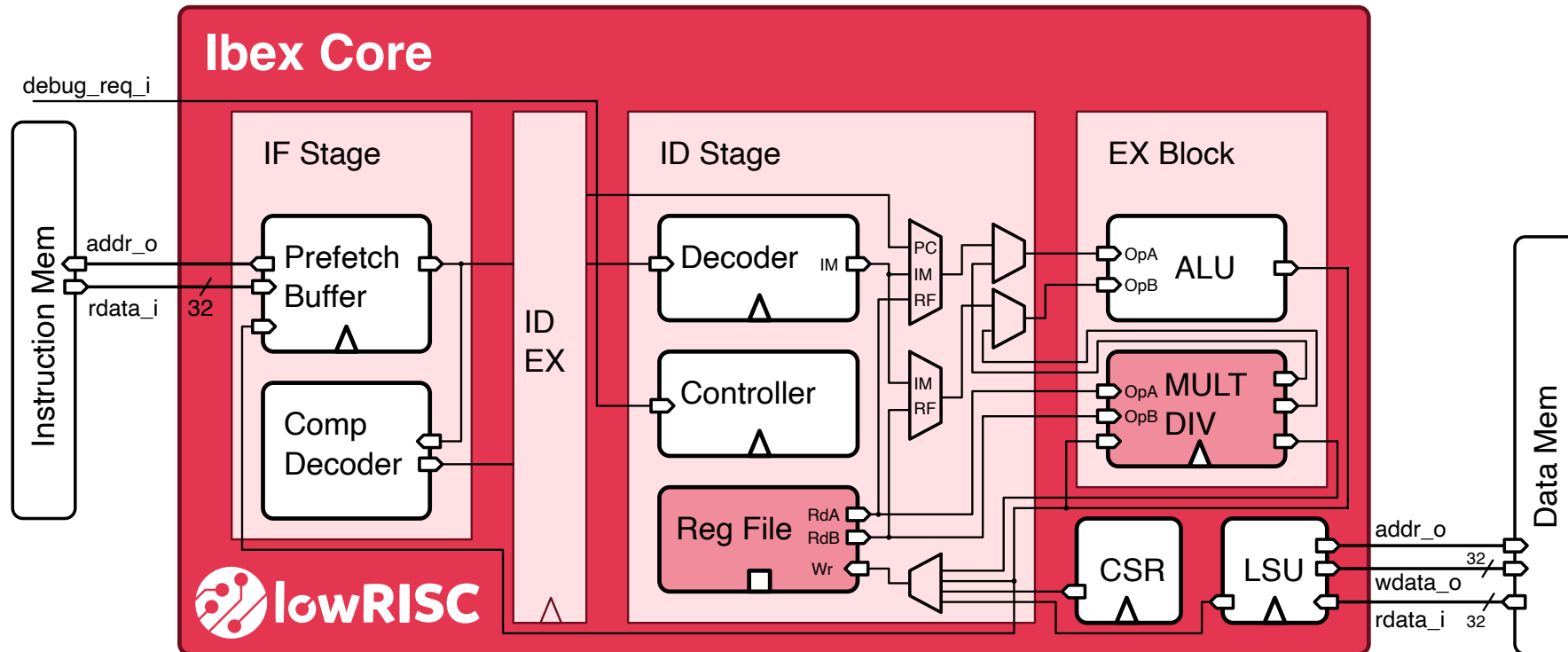
(not yet publicly released)

OpenHW RISC-V DV Flow



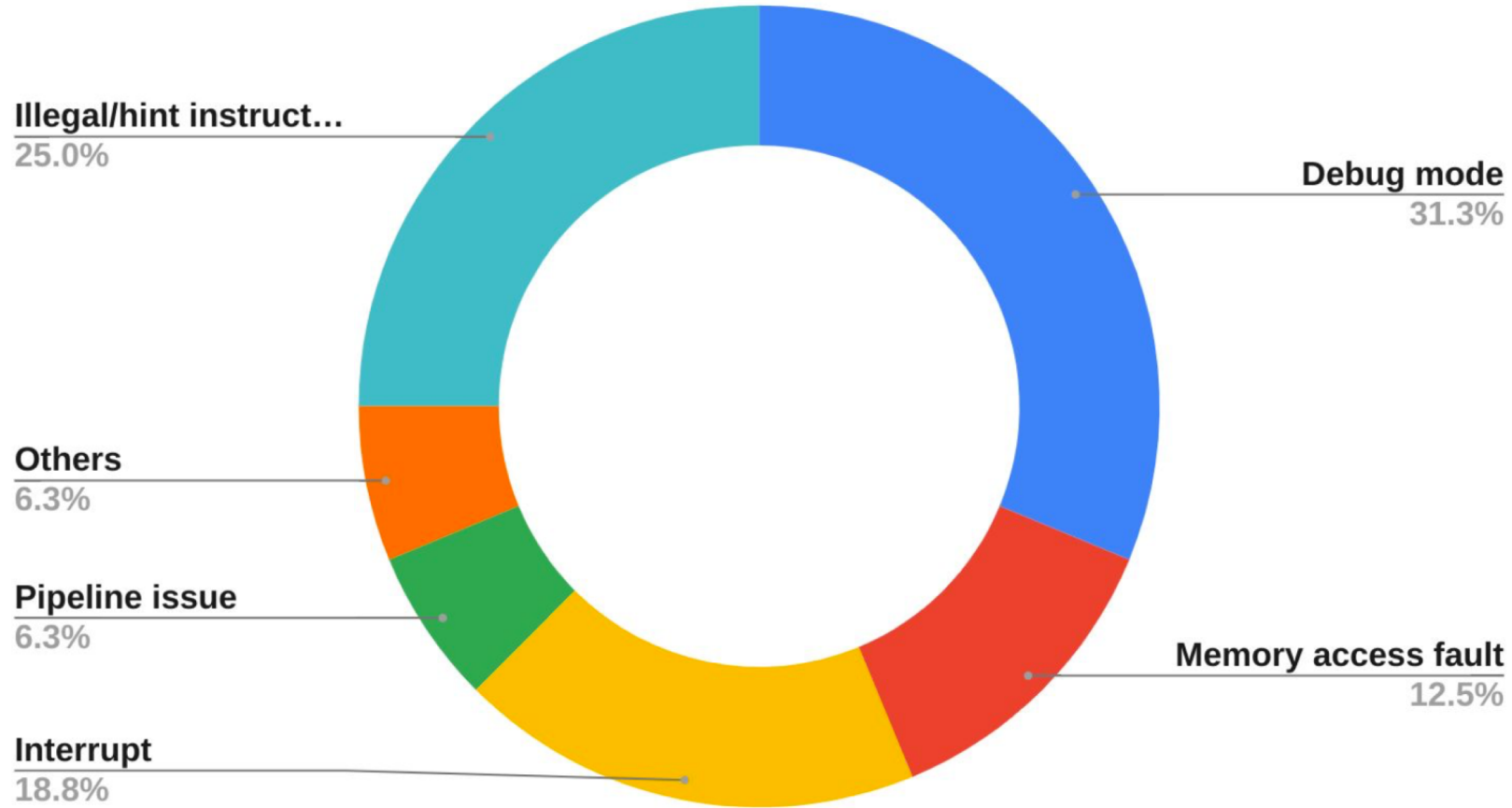
- Imperas is the RISC-V golden reference model

Case Study: lowRISC Ibex



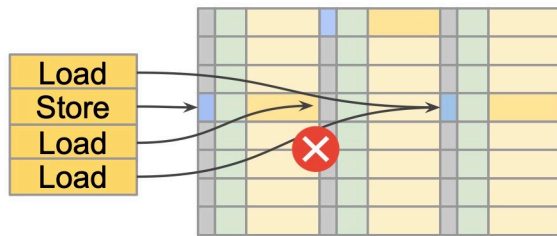
- Ibex is a small 32 bit RISC-V CPU core (RV32IMC/EMC) with a two stage pipeline, previously known as zero-risky (PULP)
- <https://github.com/lowRISC/ibex>

Case study: ibex core verification

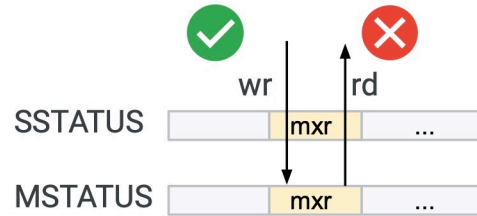


Categories of found bugs

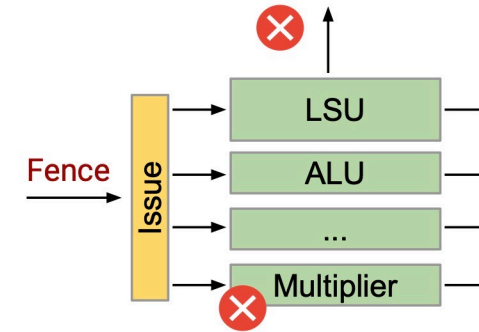
Bugs Found Using ISG Approach



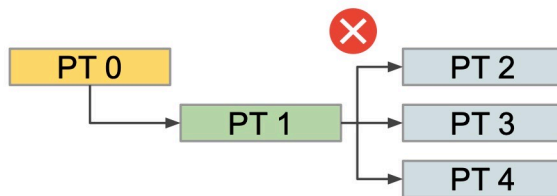
Cache line access racing



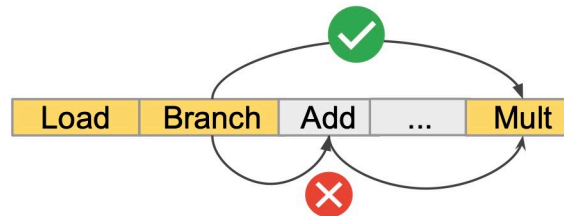
privileged CSR access



FENCE operation failure



page fault handling



Incorrect branch execution



ALU corner case bug

Image courtesy of Google LLC

Valtrix Builds Executable Test Benches

- Imperas working with Valtrix
- riscvOVPsim as reference model
- Alternative/complementary approach to Instruction Stream Generator

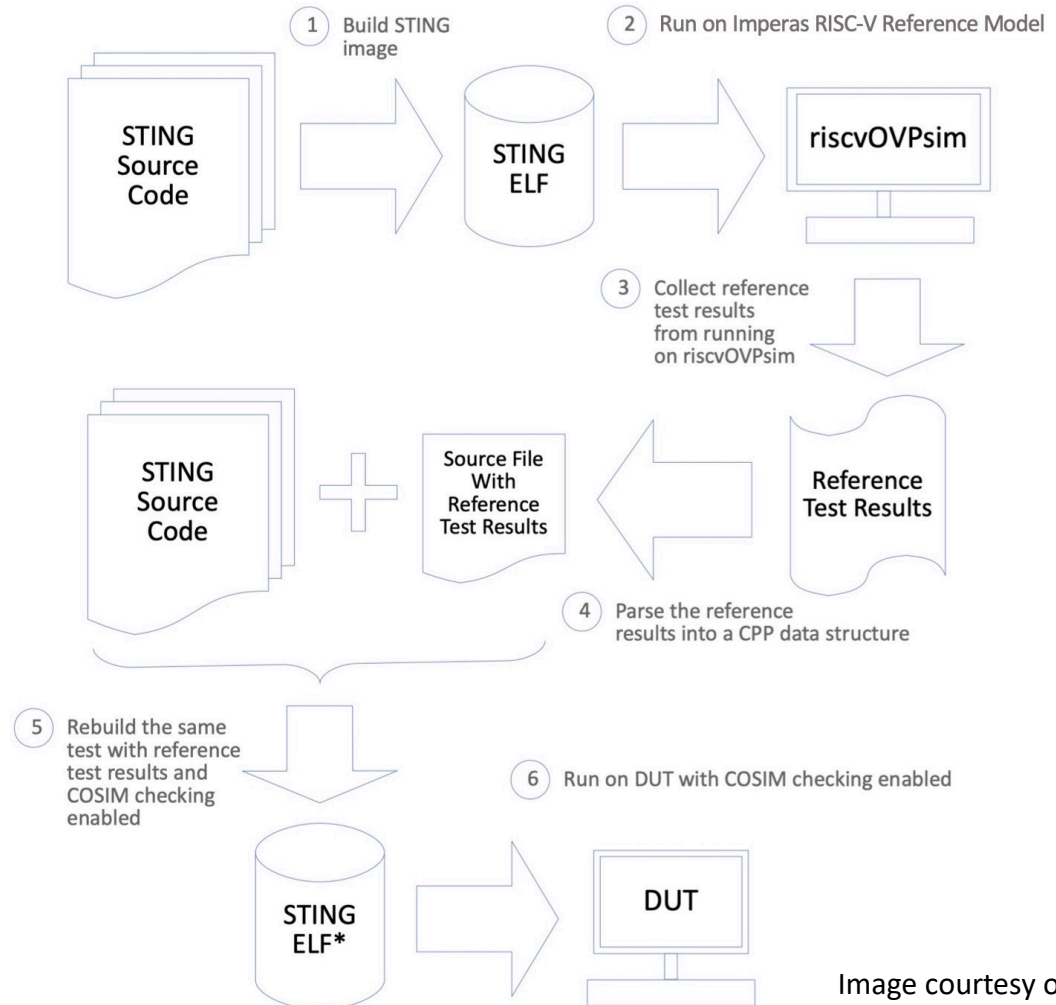


Image courtesy of Valtrix Systems

Agenda

- RISC-V verification issues
- Compliance is not verification
- Reference models and custom instructions
- Processor IP verification
- **SoC level verification**
- Summary

SoC Level Verification

- So now you have your CPU core verified...
- What about:
 - Verification of the interface between the processor or processing element and the NoC
 - Simple answer is that NoC verification IP is used
 - This takes some effort, which is taken for granted with traditional processors
 - Verification of processing elements with multiple RISC-V cores, as is common in AI/ML SoCs?
 - This flow is still evolving / being invented

Agenda

- RISC-V verification issues
- Compliance is not verification
- Reference models and custom instructions
- Processor IP verification
- SoC level verification
- **Summary**

Summary

- DV is a critical issue for RISC-V processor IP and SoCs
- Compliance testing is a subset of DV
- Reference models are needed, and are now available
- Directed testing, instruction stream generation and test generation/execution are being used for processor IP DV
- Step and compare methodology provides the most efficient DV flows
- More work is needed – the efficient DV of RISC-V processors is evolving



Thank you

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