x86: SVM AVIC

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A bit of Archeology

Xen Summit 2026

2012 (Xen Summit): Introduction of AMD Advanced Virtual Interrupt Controller

https://www.slideshare.net/slideshow/introduction-of-amd-virtual-interrupt-controller/14232698

2016: SVM AVIC v1

https://lore.kernel.org/xen-devel/1474264368-4104-1-git-send-email-suravee.suthikulpanit@amd.com/

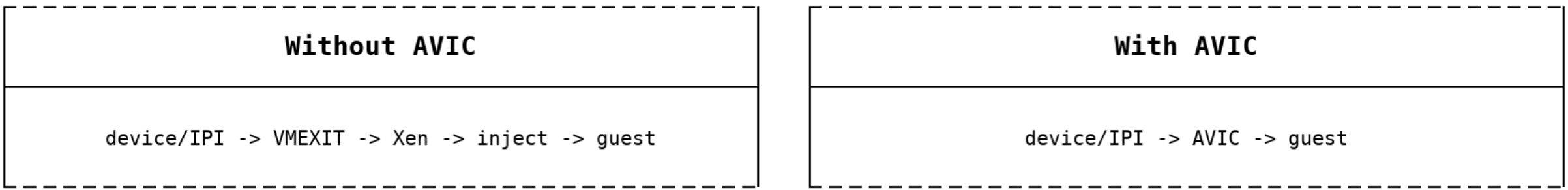
2018: SVM AVIC v2

https://lore.kernel.org/xen-devel/20180507210753.2280-1-Janakarajan.Natarajan@amd.com/

Why enable AVIC?

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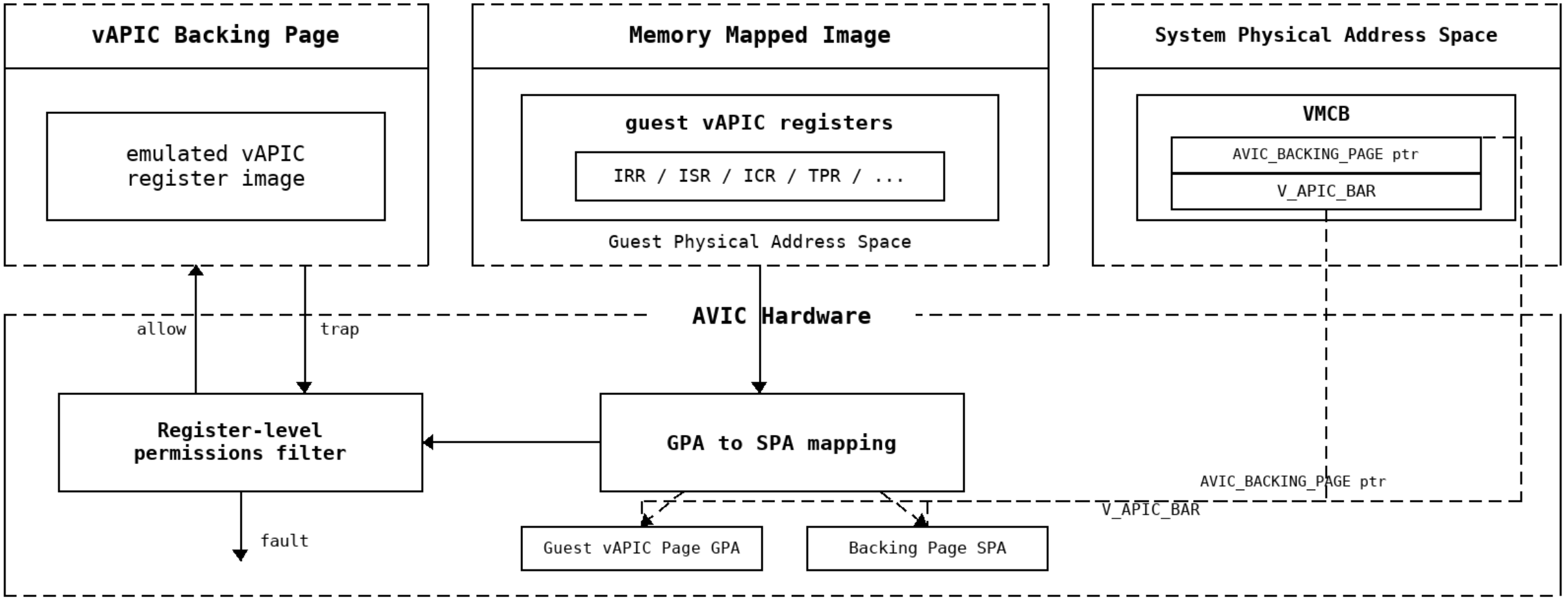
- Reduce interrupt-related VMEXITs
- Shorter interrupt path for LAPIC/IPI delivery
- Lower latency and less hypervisor overhead
- Important for scalable SMP guests and frequent timer/IPI traffic



Reduce number of VMEXITs in interrupt delivery hot paths

AVIC Backing Page

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Accelerated access: TPR, EOI, ICR

Physical and Logical APIC ID tables

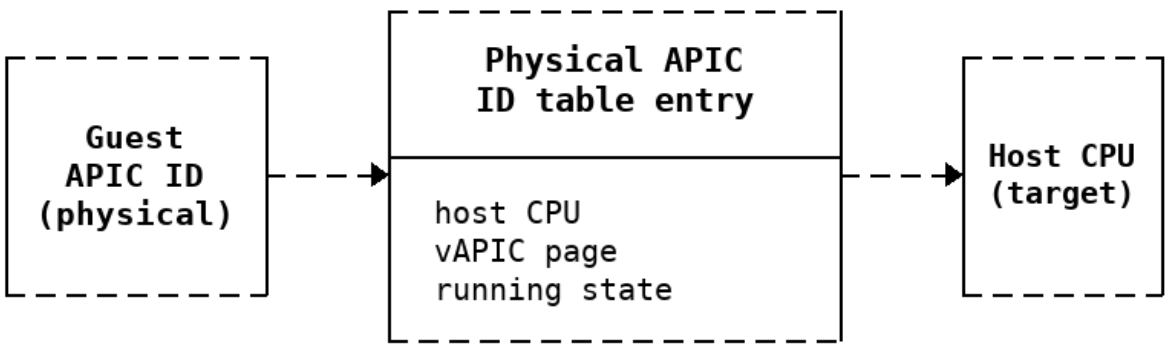
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Physical APIC ID table

- Used for hardware routing of guest physical-destination interrupts

- Entry links guest APIC ID to host CPU and vAPIC backing page

- Tracks whether the target vCPU is running

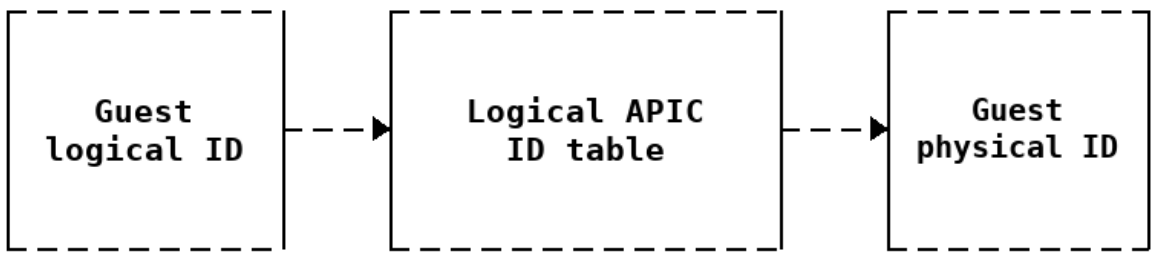


Logical APIC ID table

- Maps guest logical IDs to guest physical IDs

- Used for logically addressed IPIs

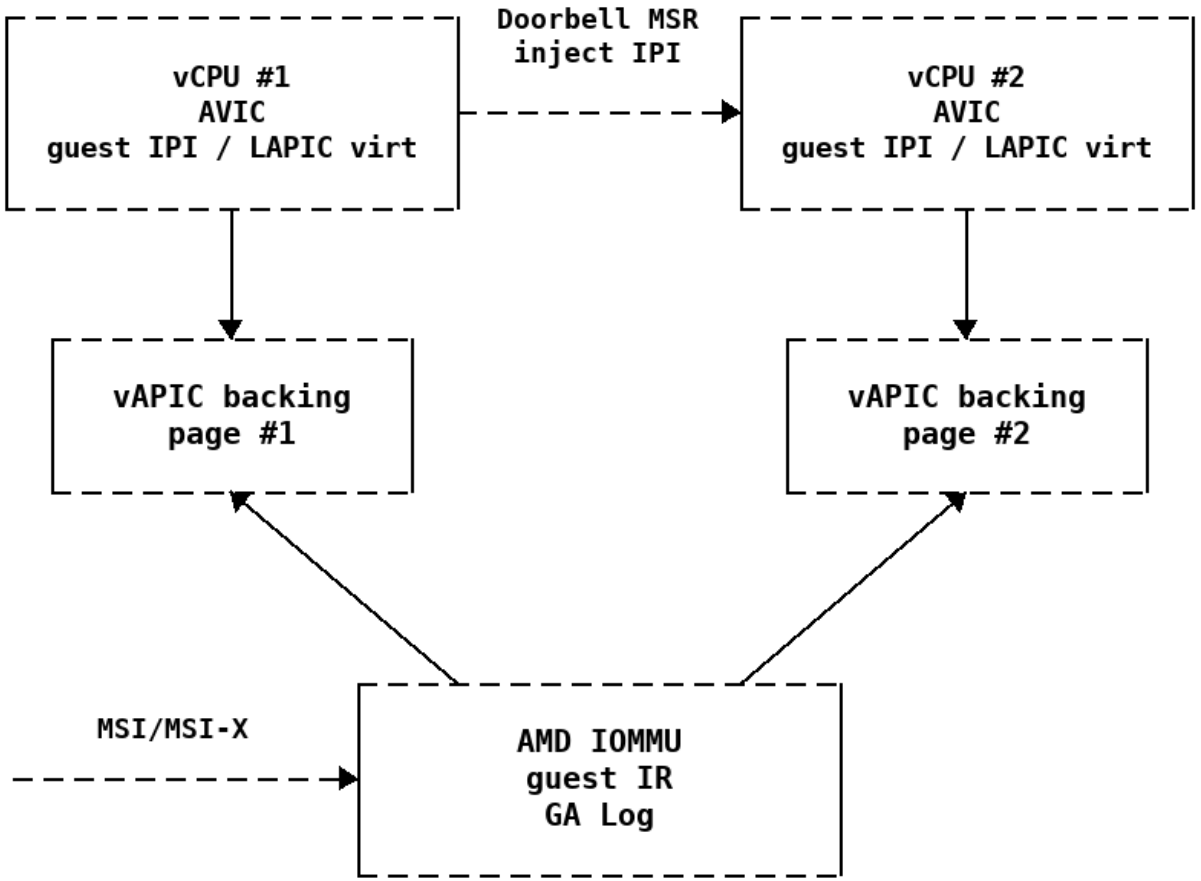
- Depends on LDR / DFR interpretation



Scheduling and migration update these mappings.

x86: Doorbell and IOMMU extension

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- Doorbell delivers guest interrupts to a specific host core

- Guest-generated IPIs, software doorbell writes, and IOMMU-remapped interrupts can all use the mechanism

- GA Log belongs to AMD IOMMU guest interrupt remapping

Xen SVM AVIC: implementation status

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Experimental branch (tip of staging):

https://gitlab.com/xen-project/people/dmukhin/xen/-/commits/svm-avic-experiment

Implemented

- [x] vAPIC backing page setup
- [x] Physical/logical ID tables
- [x] Posted interrupt delivery into IRR
- [x] Incomplete IPI handling
- [x] Initial bring-up on real hardware
- [x] Family-specific IPIV quirks (AMD erratum 1235)
- [x] Scheduler/doorbell synchronization
- [x] IPI via MSR write path

Current limitations / TODOs

- [ ] No IOMMU integration yet -> no MSI/MSI-X acceleration
- [ ] No x2APIC mode support
- [ ] No guest APIC-base relocation handling for V_APIC_BAR
- [ ] No hybrid mode (x2APIC operation in xAVIC mode)

Validation

- [x] Regression test on real hw: upstream CI targets (Zen2/Zen3)
- [ ] Add XTF IPI latency test (p50/p99/max latency w/ AVIC on/off)
- [ ] Future device-interrupt tests depend on GA Log and IOMMU support

Summary

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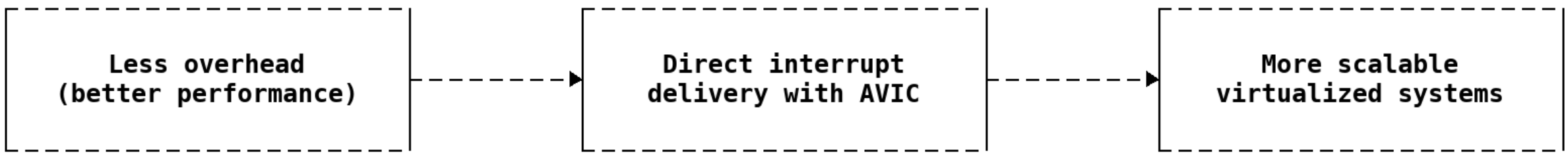
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[x] AVIC reduces APIC virtualization overhead

[x] Key structures are the backing page and APIC ID tables

[x] Doorbell and IOMMU integration are central to low-latency delivery

[x] Xen implementation works today with important limitations



Thank you!


SVM
AVIC